HI-5200

10 Base-T/100Base-TX Physical Layer Transceiver with Extended Temperature Operation

August 2021

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1. General Description

The HI-5200 is a single supply 10Base-T/100Base-TX physical layer transceiver, which provides MII/RMII interfaces to transmit and receive data.

HP Auto MDI/MDI-X provides the most robust solution for eliminating the need to differentiate between crossover and straight-through cables. An optional interrupt pin provides status updates to the external controller, avoiding the need for continuous polling.

The HI-5200 is available in 32-pin QFN (5mm x 5mm) or QFP packages. The device is capable of enhanced (−40°C to +105°C) and extended (−55°C to +125°C) operating temperature ranges.

2. Features

- Single-chip 10Base-T/100Base-TX physical layer solution with auto-negotiation
- Pin selectable 10Base-T or 100Base-Tx at power-up/reset with auto-negotiation disable option
- Fully compliant to IEEE 802.3u standard
- Low power CMOS design, power consumption of <180mW
- HP auto MDI/MDI-X for reliable detection and correction for straight-through and crossover cables with disable and enable option
- Robust operation over standard cables
- Power down and power saving modes
- MII interface support
- RMII interface support with external 50MHz system clock
- MIIM (MDC/MDIO) management bus to 6.25MHz for rapid PHY register configuration
- Interrupt pin option
- Programmable LED outputs for link, activity and speed
- ESD rating (6kV)
- Single power supply (3.3V)
- Built-in 1.8V regulator for core
- Enhanced (−40°C to +105°C) and extended (−55°C to +125°C) operating temperature ranges
- Full range of supporting magnetics available in both industrial and extended operating temperature ranges
- Available in a 32-pin QFN (5mm x 5mm) or thermally enhanced QFP packages

3. Pin Configurations (Top)

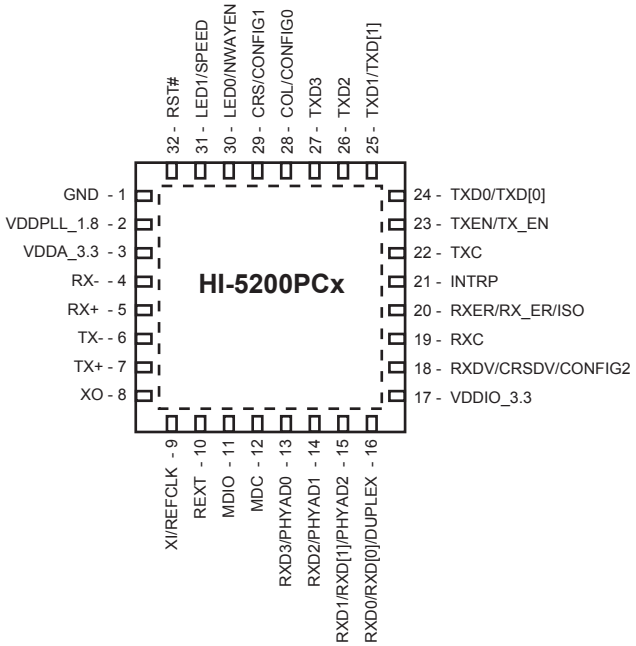


Figure 1. HI-5200: 32-Pin Plastic 5mm x 5mm QFN

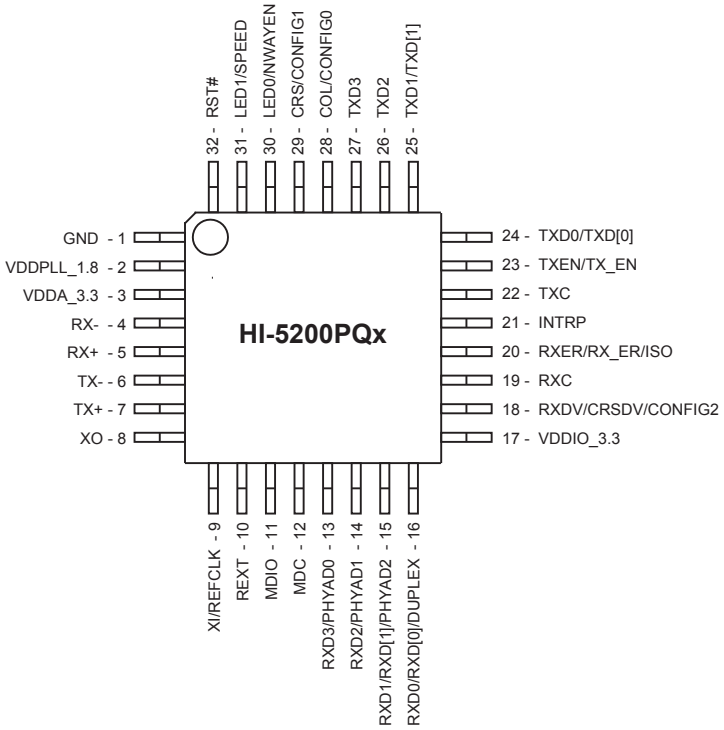


Figure 2. HI-5200: 32-Pin Plastic 9mm x 9mm TQFP

4. Block Diagram

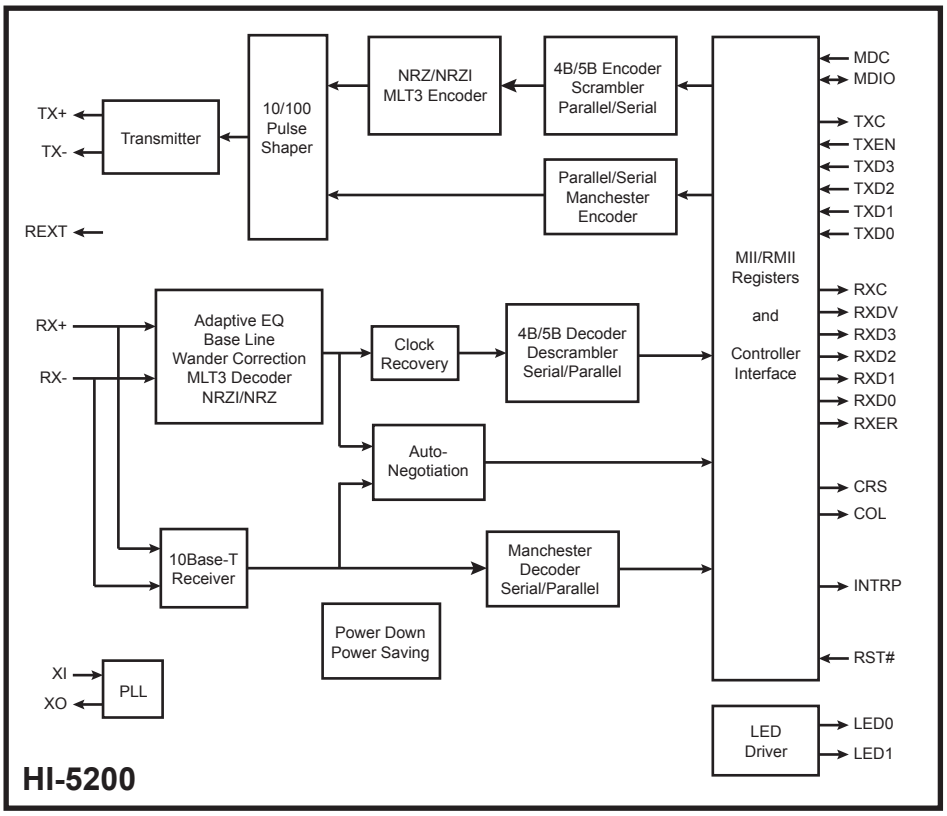


Figure 3. HI-5200 Block Diagram

5. Pin Descriptions

Table 1. HI-5200 Pin Descriptions

Pin Number	Pin Name	Function [1]	Description
1	GND	Gnd	Ground.
2	VDDPLL_1.8	P	1.8V Analog V_{DD} Decouple with 10µF and 0.1µF capacitors to ground.
3	VDDA_3.3	P	3.3V Analog V_{DD}.
4	RX-	I/O	Physical receive or transmit signal (- differential).
5	RX+	I/O	Physical receive or transmit signal (+ differential).
6	TX-	I/O	Physical transmit or receive signal (- differential).
7	TX+	I/O	Physical transmit or receive signal (+ differential).
8	XO	O	Crystal Feedback. This pin is used only in MII mode when a 25MHz crystal is used. This pin is a no connect if oscillator or external clock source is used, or if RMII mode is selected.
9	XI / REFCLK	I	Crystal / Oscillator / External Clock Input: **MII Mode:** 25MHz ± 50ppm (crystal, oscillator or external clock) **RMII Mode:** 50MHz ± 50ppm (oscillator or external clock only)
10	REXT	I/O	Set physical transmit output current. Connect a 6.49kΩ resistor in parallel with a 100pF capacitor to ground on this pin. See HI-5200 reference schematics.
11	MDIO	I/O	Management Interface (MII) Data I/O This pin requires an external 4.7kΩ pull-up resistor.
12	MDC	I	Management Interface (MII) Clock Input This pin is synchronous to the MDIO data interface.
13	RXD3 / PHYAD0	Ipu/O	**MII Mode:** Receive Data Output[3][2]. **Config Mode:** The pull-up/pull-down value is latched as PHYADDR[0] during power-up / reset. See “Strapping Options” for details.
14	RXD2 / PHYAD1	Ipd/O	**MII Mode:** Receive Data Output[2][2]. **Config Mode:** The pull-up/pull-down value is latched as PHYADDR[1] during power-up / reset. See “Strapping Options” for details.
15	RXD1 / RXD[1] / PHYAD2	Ipd/O	**MII Mode:** Receive Data Output[1][2]. **RMII Mode:** Receive Data Output[1][3]. **Config Mode:** The pull-up/pull-down value is latched as PHYADDR[2] during power-up / reset. See “Strapping Options” for details.

Pin Number	Pin Name	Function [1]	Description
16	RXD0 / RXD[0] / DUPLEX	Ipu/O	**MII Mode:** Receive Data Output[0][2]. **RMII Mode:** Receive Data Output[0][3]. **Config Mode:** Latched as DUPLEX (register 0h, bit 8) during power-up / reset. See “Strapping Options” for details.
17	VDDIO_3.3	P	3.3V Digital V_{DD}.
18	RXDV / CRSDV / CONFIG2	Ipd/O	**MII Mode:** Receive Data Valid Output. **RMII Mode:** Carrier Sense/Receive Data Valid Output. **Config Mode:** The pull-up/pull-down value is latched as CONFIG2 during power-up / reset. See “Strapping Options” for details.
19	RXC	O	**MII Mode:** Receive Clock Output.
20	RXER / RX_ER / ISO	Ipd/O	**MII Mode:** Receive Error Output. **RMII Mode:** Receive Error Output. **Config Mode:** The pull-up/pull-down value is latched as ISOLATE during power-up / reset. See “Strapping Options” for details.
21	INTRP	Opu	Programmable Interrupt Output Register 1Bh is the Interrupt Control/Status Register for programming the interrupt conditions and reading the interrupt status. Register 1Fh bit 9 sets the interrupt output to active low (default) or active high.
22	TXC	O	**MII Mode:** Transmit Clock Output.
23	TXEN / TX_EN	I	**MII Mode:** Transmit Enable Input. **RMII Mode:** Transmit Enable Input.
24	TXD0 / TXD[0]	I	**MII Mode:** Transmit Data Input[0][4]. **RMII Mode:** Transmit Data Input[0][5].
25	TXD1 / TXD[1]	I	**MII Mode:** Transmit Data Input[1][4]. **RMII Mode:** Transmit Data Input[1][5].
26	TXD2	I	**MII Mode:** Transmit Data Input[2][4]. Connect to GND in RMII Mode.
27	TXD3	I	**MII Mode:** Transmit Data Input[3][4]. Connect to GND in RMII Mode.
29	COL / CONFIG0	Ipd/O	**MII Mode:** Collision Detect Output. **Config Mode:** The pull-up/pull-down value is latched as CONFIG0 during power-up / reset. See “Strapping Options” for details.
29	CRS / CONFIG1	Ipd/O	**MII Mode:** Carrier Sense Output. **Config Mode:** The pull-up/pull-down value is latched as CONFIG1 during power-up / reset. See “Strapping Options” for details.

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Function (1)</th><th>Description</th></tr>
<tr><td>30</td><td>LED0 /
NWAYEN</td><td>Ipu/O</td><td>
LED Mode: Programmable LED0 Output.

Config Mode: Latched as Auto-Negotiation Enable (register 0h, bit 12) during power-up / reset. See “Strapping Options” for details.

The LED0 pin is programmable via register 1Eh bits [15:14], and is defined as follows:

<table>
<tr><th colspan="3">LED Mode = [00] (register 1Eh [15:14] = [0:0])</th></tr>
<tr><th>Link/Activity</th><th>LED0 Pin State</th><th>LED Definition</th></tr>
<tr><td>No Link</td><td>H</td><td>OFF</td></tr>
<tr><td>Link</td><td>L</td><td>ON</td></tr>
<tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr>
</table>

<table>
<tr><th colspan="3">LED Mode = [01] (register 1Eh [15:14] = [0:1])</th></tr>
<tr><th>Link</th><th>LED0 Pin State</th><th>LED Definition</th></tr>
<tr><td>No Link</td><td>H</td><td>OFF</td></tr>
<tr><td>Link</td><td>L</td><td>ON</td></tr>
</table>

LED Mode = [10] or [11]
Reserved.
</td></tr>
<tr><td>31</td><td>LED1 /
SPEED</td><td>Ipu/O</td><td>
LED Mode: Programmable LED1 Output /

Config Mode: Latched as SPEED (register 0h, bit 13) during power-up / reset. See “Strapping Options” for details.

The LED1 pin is programmable via register 1Eh bits [15:14], and is defined as follows:

<table>
<tr><th colspan="3">LED Mode = [00] (register 1Eh [15:14] = [0:0])</th></tr>
<tr><th>Speed</th><th>LED1 Pin State</th><th>LED Definition</th></tr>
<tr><td>10BT</td><td>H</td><td>OFF</td></tr>
<tr><td>100BT</td><td>L</td><td>ON</td></tr>
</table>

<table>
<tr><th colspan="3">LED Mode = [01] (register 1Eh [15:14] = [0:1])</th></tr>
<tr><th>Activity</th><th>LED1 Pin State</th><th>LED Definition</th></tr>
<tr><td>No Activity</td><td>H</td><td>OFF</td></tr>
<tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr>
</table>

LED Mode = [10] or [11]
Reserved.
</td></tr>
<tr><td>32</td><td>RST#</td><td>I</td><td>Chip Reset (active low).</td></tr>
<tr><td>PACKAGE
PADDLE</td><td>GND</td><td>Gnd</td><td>Ground.</td></tr>
</table>

Notes:

1. P = Power supply.
   Gnd = Ground.
   I = Input.
   O = Output.
   I/O = Bi-directional.
   Opu = Output with internal pull-up (40K ± 30%).
   Ipu/O = Input with internal pull-up (40K ± 30%) during power-up/reset; output pin otherwise.
   Ipd/O = Input with internal pull-down (40K ± 30%) during power-up/reset; output pin otherwise.
2. MII Rx Mode: The RXD[3..0] bits are synchronous with RXCLK. When RXDV is asserted, RXD[3..0] presents valid data to MAC through the MII. RXD[3..0] is invalid when RXDV is de-asserted.
3. RMII Rx Mode: The RXD[1:0] bits are synchronous with REF_CLK. For each clock period in which CRS_DV is asserted, two bits of recovered data are sent from the PHY.
4. MII Tx Mode: The TXD[3..0] bits are synchronous with TXCLK. When TXEN is asserted, TXD[3..0] presents valid data from the MAC through the MII. TXD[3..0] has no effect when TXEN is de-asserted.
5. RMII Tx Mode: The TXD[1:0] bits are synchronous with REF_CLK. For each clock period in which TX_EN is asserted, two bits of data are received by the PHY from the MAC.

5.1. Strapping Options

Pin strap-ins are latched during power-up or reset. In some systems, the MAC receive input pins may drive high during power-up or reset, and consequently cause the PHY strap-in pins on the MII/RMII signals to be latched high. In this case, it is recommended to add 1K pull-downs on these PHY strap-in pins to ensure the PHY does not strap-in to ISOLATE mode, or is not configured with an incorrect PHY Address.

Table 2. HI-5200 Strapping Options

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Function (1)</th><th>Description</th></tr>
<tr><td>15</td><td>PHYAD2</td><td>Ipd/O</td><td rowspan="3">The PHY Address is latched at power-up / reset and is configurable to any value from 1 to 7.
The default PHY Address is 00001.
PHY Address bits [4:3] are always set to ‘00’.</td></tr>
<tr><td>14</td><td>PHYAD1</td><td>Ipd/O</td></tr>
<tr><td>13</td><td>PHYAD0</td><td>Ipd/O</td></tr>
<tr><td>18</td><td>CONFIG2</td><td>Ipd/O</td><td rowspan="4">The CONFIG[2:0] strap-in pins are latched at power-up / reset and are defined as follows:
<table><tr><th>CONFIG[2:0]</th><th>Mode</th></tr><tr><td>000</td><td>MII (default)</td></tr><tr><td>001</td><td>RMII</td></tr><tr><td>010</td><td>Reserved − not used</td></tr><tr><td>011</td><td>Reserved − not used</td></tr><tr><td>100</td><td>MII 100Mbps Preamble Restore</td></tr><tr><td>101</td><td>Reserved − not used</td></tr><tr><td>110</td><td>Reserved − not used</td></tr><tr><td>111</td><td>Reserved − not used</td></tr></table></td></tr>
<tr><td>29</td><td>CONFIG1</td><td>Ipd/O</td></tr>
<tr><td>28</td><td>CONFIG0</td><td>Ipd/O</td></tr>
</table>

Pin Number	Pin Name	Function [1]	Description
20	ISO	Ipd/O	ISOLATE Mode: Pull-up = Enable Pull-down (default) = Disable During power-up / reset, this pin value is latched into register 0h bit 10.
31	SPEED	Ipu/O	SPEED Mode: Pull-up (default) = 100Mbps Pull-down = 10Mbps During power-up / reset, this pin value is latched into register 0h bit 13 as the Speed Select, and also is latched into register 4h (Auto-Negotiation Advertisement) as the Speed capability support.
16	DUPLEX	Ipu/O	DUPLEX Mode: Pull-up (default) = Half Duplex Pull-down = Full Duplex During power-up / reset, this pin value is latched into register 0h bit 8 as the Duplex Mode.
30	NWAYEN	Ipu/O	Nway Auto-Negotiation Enable Pull-up (default) = Enable Auto-Negotiation Pull-down = Disable Auto-Negotiation During power-up / reset, this pin value is latched into register 0h bit 12.

Notes:

1. Ipu/O = Input with internal pull-up (40K ± 30%) during power-up/reset; output pin otherwise.
   Ipd/O = Input with internal pull-down (40K ± 30%) during power-up/reset; output pin otherwise.

6. Functional Description

The HI-5200 is a single 3.3V supply Fast Ethernet transceiver. It is fully compliant with the IEEE 802.3u Specification.

The device supports 10Base-T and 100Base-TX with HP auto MDI/MDI-X for reliable detection of and correction for straight-through and crossover cables.

The HI-5200 offers a choice of MII or RMII data interface connection with the MAC processor. The MII management bus option gives the MAC processor complete access to the HI-5200 control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll for PHY status changes.

Physical signal transmission and reception are enhanced through the use of patented analog circuitries that make the design more efficient and allow for lower power consumption and smaller chip die size.

6.1. 100Base-TX Transmit

The 100Base-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output.

The output current is set by an external 6.49kΩ 1% resistor for the 1:1 transformer ratio. It has typical rise/fall times of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot and timing jitter. The wave-shaped 10Base-T output drivers are also incorporated into the 100Base-TX drivers.

6.2. 100Base-TX Receive

The 100Base-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

6.3. PLL Clock Synthesizer

The HI-5200 generates 125MHz, 25MHz and 20MHz clocks for system timing. Internal clocks are generated from an external 25MHz crystal or oscillator. For the HI-5200 in RMII mode, these internal clocks are generated from an external 50MHz oscillator or system clock.

6.4. Scrambler/De-Scrambler (100Base-TX only)

The purpose of the scrambler is to spread the power spectrum of the signal in order to reduce EMI and baseline wander.

6.5. 10Base-T Transmit

The 10Base-T drivers are incorporated with the 100Base-TX drivers to allow for transmission using the same magnetics. The drivers also perform internal wave-shaping and pre-emphasize, and output 10Base-T signals with a typical amplitude of 2.5V peak. The 10Base-T signals have harmonic contents that are at least 27dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

6.6. 10Base-T Receive

On the receive side, input buffer and level detecting squelch circuits are employed. A differential input receiver circuit and a PLL performs the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400mV or with short pulse widths to prevent noise at the RX+ and RX- inputs from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the HI-5200 decodes a data frame. The receive clock is kept active during idle periods in between data reception.

6.7. SQE and Jabber Function (10Base-T only)

In 10Base-T operation, a short pulse is put out on the COL pin after each frame is transmitted. This SQE Test is required as a test of the 10Base-T transmit/receive path. If transmit enable (TXEN) is high for more than 20ms (jabbering), the 10Base-T transmitter is disabled and COL is asserted high. If TXEN is then driven low for more than 250ms, the 10Base-T transmitter is re-enabled and COL is de-asserted (returns to low).

6.8. Auto-Negotiation

The HI-5200 conforms to the auto-negotiation protocol, defined in Clause 28 of the IEEE 802.3u specification. Auto-negotiation is enabled by either hardware pin strapping (pin 30) or software (register 0h bit 12).

Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the highest common mode of operation. Link partners advertise their capabilities to each other, and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the mode of operation.

The following list shows the speed and duplex operation mode from highest to lowest.

- Priority 1: 100Base-TX, full-duplex
- Priority 2: 100Base-TX, half-duplex
- Priority 3: 10Base-T, full-duplex
- Priority 4: 10Base-T, half-duplex

If auto-negotiation is not supported or the HI-5200 link partner is forced to bypass auto-negotiation, the HI-5200 sets its operating mode by observing the signal at its receiver. This is known as parallel detection, and allows the HI-5200 to establish link by listening for a fixed signal protocol in the absence of auto-negotiation advertisement protocol.

The auto-negotiation link up process is shown in the flow chart illustrated in Figure 4.

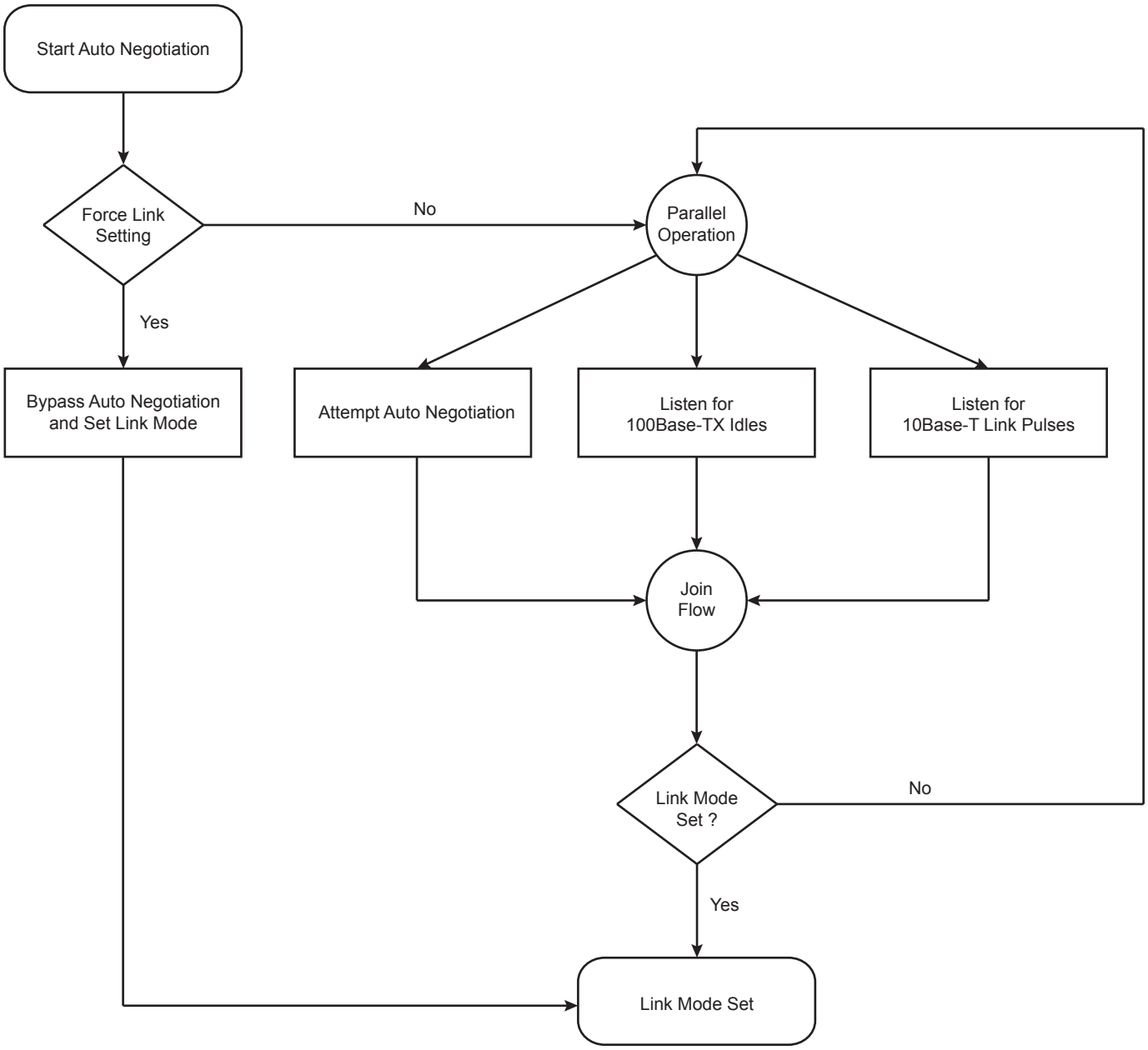


Figure 4. Auto Negotiation Flow Chart

6.9. MII Management (MIIM) Interface

The HI-5200 supports the IEEE 802.3 MII Management Interface, also known as the Management Data Input / Output (MDIO) Interface. This interface allows upper-layer devices to monitor and control the state of the HI-5200. An external device with MIIM capability is used to read the PHY status and/or configure the PHY settings. Further details on the MIIM interface can be found in Clause 22.2.4 of the IEEE 802.3 Specification.

The MIIM interface consists of the following:

- A physical connection that incorporates the clock line (MDC) and the data line (MDIO).
- A specific protocol that operates across the aforementioned physical connection that allows a external controller to communicate with one or more PHY devices. Each HI-5200 device is assigned a unique PHY address between 1 and 7 by its PHYAD[2:0] strapping pins. Also, every device supports the broadcast PHY address 0, as defined per the IEEE 802.3 Specification, which can be used to read/write to a single device, or write to multiple HI-5200 devices simultaneously.
- A set of 16-bit MDIO registers. Register [0:6] are required, and their functions are defined per the IEEE 802.3 Specification. The additional registers are provided for expanded functionality.

Table 3 shows the MII Management frame format for the HI-5200.

Table 3. MII Management Frame Format

	Preamble	Start of Frame	Read/Write Op Code	PHY Address Bits [4:0]	REG Address Bits [4:0]	TA	Data Bits [15:0]	Idle
Read	32 1's	01	10	00AAA	RRRRR	Z0	DDDDDDDD_DDDDDDDD	Z
Write	32 1's	01	01	00AAA	RRRRR	10	DDDDDDDD_DDDDDDDD	Z

6.10. Interrupt (INTRP)

INTRP (pin 21) is an optional interrupt signal that is used to inform the external controller that there has been a status update to the PHY registers. Bits[15:8] of register 1Bh are the interrupt control bits, and are used to enable and disable the conditions for asserting the INTRP signal. Bits[7:0] of register 1Bh are the interrupt status bits, and are used to indicate which interrupt conditions have occurred. The interrupt status bits are cleared after reading register 1Bh.

Bit 9 of register 1Fh sets the interrupt level to active high or active low.

6.11. MII Data Interface

The Media Independent Interface (MII) is specified in Clause 22 of the IEEE 802.3 Specification. It provides a common interface between physical layer and MAC layer devices, and has the following key characteristics:

- Supports 10Mbps and 100Mbps data rates.
- Uses a 25MHz reference clock, sourced by the PHY.
- Provides independent 4-bit wide (nibble) transmit and receive data paths.
- Contains two distinct groups of signals: one for transmission and the other for reception.

The HI-5200 is configured to MII mode after it is power-up or reset with the following:

- A 25MHz crystal connected to XI, XO (pins 9, 8), or an external 25MHz clock source (oscillator) connected to XI.
- CONFIG[2:0] (pins 18, 29, 28) set to '000' (default setting).

6.12. MII Signal Definition

Table 4 describes the MII signals. Refer to Clause 22 of the IEEE 802.3 Specification for detailed information.

Table 4. MII Signal Definition

MII Signal Name	Direction (with respect to PHY, HI-5200 signal)	Direction (with respect to MAC)	Description
TXC	Output	Input	Transmit Clock (2.5MHz for 10Mbps; 25MHz for 100Mbps)
TXEN	Input	Output	Transmit Enable
TXD[3:0]	Input	Output	Transmit Data [3:0]
RXC	Output	Input	Receive Clock (2.5MHz for 10Mbps; 25MHz for 100Mbps)
RXDV	Output	Input	Receive Data Valid
RXD[3:0]	Output	Input	Receive Data [3:0]
RXER	Output	Input or (not required)	Receive Error
CRS	Output	Input	Carrier Sense
COL	Output	Input	Collision Detection

6.12.1. Transmit Clock (TXC)

TXC is sourced by the PHY. It is a continuous clock that provides the timing reference for TXEN and TXD[3:0].

TXC is 2.5MHz for 10Mbps operation and 25MHz for 100Mbps operation.

6.12.2. Transmit Enable (TXEN)

TXEN indicates the MAC is presenting nibbles on TXD[3:0] for transmission. It is asserted synchronously with the first nibble of the preamble and remains asserted while all nibbles to be transmitted are presented on the MII, and is negated prior to the first TXC following the final nibble of a frame.

TXEN transitions synchronously with respect to TXC.

6.12.3. Transmit Data [3:0] (TXD[3:0])

TXD[3:0] transitions synchronously with respect to TXC. When TXEN is asserted, TXD[3:0] are accepted for transmission by the PHY. TXD[3:0] is “00” to indicate idle when TXEN is de-asserted. Values other than “00” on TXD[3:0] while TXEN is de-asserted are ignored by the PHY.

6.12.4. Receive Clock (RXC)

RXC provides the timing reference for RXDV, RXD[3:0], and RXER.

- In 10Mbps mode, RXC is recovered from the line while carrier is active. RXC is derived from the PHY's reference clock when the line is idle, or link is down.
- In 100Mbps mode, RXC is continuously recovered from the line. If link is down, RXC is derived from the PHY's reference clock.

RXC is 2.5MHz for 10Mbps operation and 25MHz for 100Mbps operation.

6.12.5. Receive Data Valid (RXDV)

RXDV is driven by the PHY to indicate that the PHY is presenting recovered and decoded nibbles on RXD[3:0].

- In 10Mbps mode, RXDV is asserted with the first nibble of the SFD (Start of Frame Delimiter), "5D", and remains asserted until the end of the frame.
- In 100Mbps mode, RXDV is asserted from the first nibble of the preamble to the last nibble of the frame. RXDV transitions synchronously with respect to RXC.

6.12.6. Receive Data [3:0] (RXD[3:0])

RXD[3:0] transitions synchronously with respect to RXC. For each clock period in which RXDV is asserted, RXD[3:0] transfers a nibble of recovered data from the PHY.

6.12.7. Receive Error (RXER)

RXER is asserted for one or more RXC periods to indicate that a Symbol Error (e.g. a coding error that a PHY is capable of detecting, and that may otherwise be undetectable by the MAC sub-layer) was detected somewhere in the frame presently being transferred from the PHY.

RXER transitions synchronously with respect to RXC. While RXDV is de-asserted, RXER has no effect on the MAC.

6.12.8. Carrier Sense (CRS)

CRS is asserted and de-asserted as follows:

- In 10Mbps mode, CRS assertion is based on the reception of valid preambles. CRS de-assertion is based on the reception of an end-of-frame (EOF) marker.
- In 100Mbps mode, CRS is asserted when a start-of-stream delimiter, or /J/K symbol pair is detected. CRS is de-asserted when an end-of-stream delimiter, or /T/R symbol pair is detected. Additionally, the PMA layer de-asserts CRS if IDLE symbols are received without /T/R.

6.12.9. Collision (COL)

COL is asserted in half-duplex mode whenever the transmitter and receiver are simultaneously active on the line. This is used to inform the MAC that a collision has occurred during its transmission to the PHY.

COL transitions asynchronously with respect to TXC and RXC.

6.13. Reduced MII (RMII) Data Interface

The Reduced Media Independent Interface (RMII) specifies a low pin count Media Independent Interface (MII). It provides a common interface between physical layer and MAC layer devices, and has the following key characteristics:

- Supports 10Mbps and 100Mbps data rates.
- Uses a 50MHz reference clock.
- Provides independent 2-bit wide (di-bit) transmit and receive data paths.
- Contains two distinct groups of signals: one for transmission and the other for reception.

The HI-5200 is configured in RMII mode after it is power-up or reset with the following:

- A 50MHz reference clock connected to REFCLK (pin 9).
- CONFIG[2:0] (pins 18, 29, 28) set to '001'.

In RMII mode, unused MII signals, TXD3 and TXD2 (pins 27 and 26 respectively), are tied to ground.

6.14. RMII Signal Definition

Table 5 describes the RMII signals for HI-5200. Refer to RMII Specification for detailed information.

Table 5. HI-5200 RMII Signal Definition

RMII Signal Name	Direction (with respect to PHY, HI-5200 signal)	Direction (with respect to MAC)	Description
REFCLK	Input	Input or Output	Synchronous 50 MHz clock reference for receive, transmit and control interface
TXEN	Input	Output	Transmit Enable
TXD[1:0]	Input	Output	Transmit Data [1:0]
CRSDV	Output	Input	Carrier Sense/Receive Data Valid
RXD[1:0]	Output	Input	Receive Data [1:0]
RXER	Output	Input or (not required)	Receive Error

6.14.1. Reference Clock (REFCLK)

REFCLK is a continuous 50MHz clock input that provides the timing reference for TXEN, TXD[1 :0], CRSDV, RXD[1:0], and RXER.

The 50MHz REFCLK input may come from the MAC or system board (see Figure 5).

6.14.2. Transmit Enable (TXEN)

TXEN indicates that the MAC is presenting di-bits on TXD[1:0] for transmission. It is asserted synchronously with the first nibble of the preamble and remains asserted while all di-bits to be transmitted are presented on the RMII, and is negated prior to the first REFCLK following the final di-bit of a frame.

TXEN transitions synchronously with respect to REFCLK.

6.14.3. Transmit Data [1:0] (TXD[1:0])

TXD[1:0] transitions synchronously with respect to REFCLK. When TXEN is asserted, TXD[1:0] are accepted for transmission by the PHY. TXD[1:0] is “00” to indicate idle when TXEN is de-asserted. Values other than “00” on TXD[1:0] while TXEN is de-asserted are ignored by the PHY.

6.14.4. Carrier Sense/Receive Data Valid (CRSDV)

CRSDV is asserted by the PHY when the receive medium is non-idle. It is asserted asynchronously on detection of carrier. This is when squelch is passed in 10Mbps mode, and when 2 non-contiguous zeroes in 10 bits are detected in 100Mbps mode. Loss of carrier results in the de-assertion of CRSDV.

So long as carrier detection criteria are met, CRSDV remains asserted continuously from the first recovered di-bit of the frame through the final recovered di-bit, and it is negated prior to the first REFCLK that follows the final di-bit. The data on RXD[1:0] is considered valid once CRSDV is asserted. However, since the assertion of CRSDV is asynchronous relative to REFCLK, the data on RXD[1:0] is “00” until proper receive signal decoding takes place.

6.14.5. Receive Data [1:0] (RXD[1:0])

RXD[1:0] transitions synchronously to REFCLK. For each clock period in which CRSDV is asserted, RXD[1:0] transfers two bits of recovered data from the PHY. RXD[1:0] is “00” to indicate idle when CRSDV is de-asserted. Values other than “00” on RXD[1:0] while CRSDV is de-asserted are ignored by the MAC.

6.14.6. Receive Error (RXER)

RXER is asserted for one or more REFCLK periods to indicate that a Symbol Error (e.g. a coding error that a PHY is capable of detecting, and that may otherwise be undetectable by the MAC sub-layer) was detected somewhere in the frame presently being transferred from the PHY.

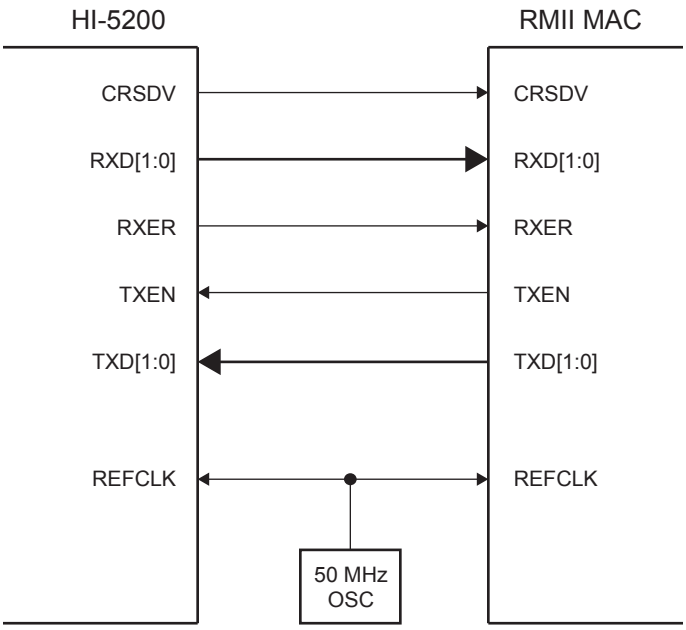
RXER transitions synchronously with respect to REFCLK. While CRSDV is de-asserted, RXER has no effect on the MAC.

6.14.7. Collision Detection

The MAC regenerates the COL signal of the MII from TXEN and CRSDV.

6.15. RMII Signal Diagram

The HI-5200 RMII pin connections to the MAC are shown in Figure 5.



OR

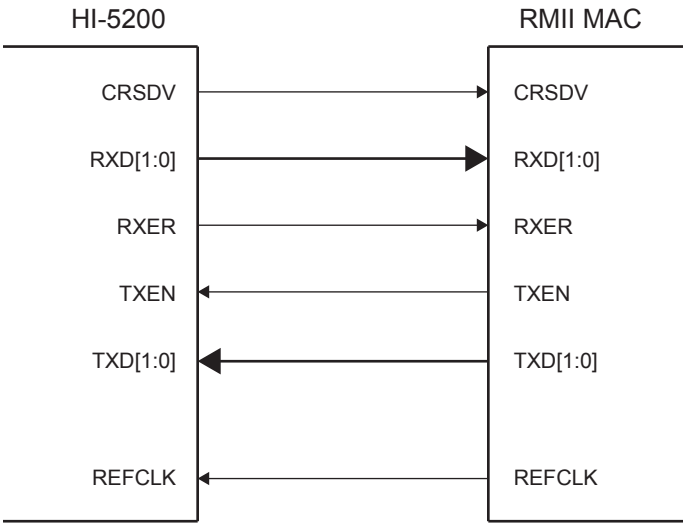


Figure 5. HI-5200 RMII Interface

6.16. HP Auto MDI/MDI-X

HP Auto MDI/MDI-X configuration eliminates the confusion of whether to use a straight cable or a crossover cable between the HI-5200 and its link partner. This feature allows the device to use either type of cable to connect with a link partner that is in either MDI or MDI-X mode. The auto-sense function detects transmit and receive pairs from the link partner, and then assigns transmit and receive pairs of the HI-5200 accordingly.

HP Auto MDI/MDI-X is enabled by default. It is disabled by writing a one to register 1Fh bit 13. MDI and MDI-X mode is selected by register 1Fh bit 14 if HP Auto MDI/MDI-X is disabled.

An isolation transformer with symmetrical transmit and receive data paths is recommended to support auto MDI/MDI-X. The IEEE 802.3 Standard defines MDI and MDI-X as shown in Table 6:

Table 6. MDI/MDI-X Pin Description

MDI		MDI-X	
RJ-45 Pin	**Signal**	**RJ-45 Pin**	**Signal**
1	TD+	1	RD+
2	TD-	2	RD-
3	RD+	3	TD+
6	RD-	6	TD-

6.16.1. Straight Cable

A straight cable connects a MDI device to a MDI-X device, or a MDI-X device to a MDI device. Figure 6 depicts a typical straight cable connection between a NIC card (MDI) and a switch, or hub (MDI-X).

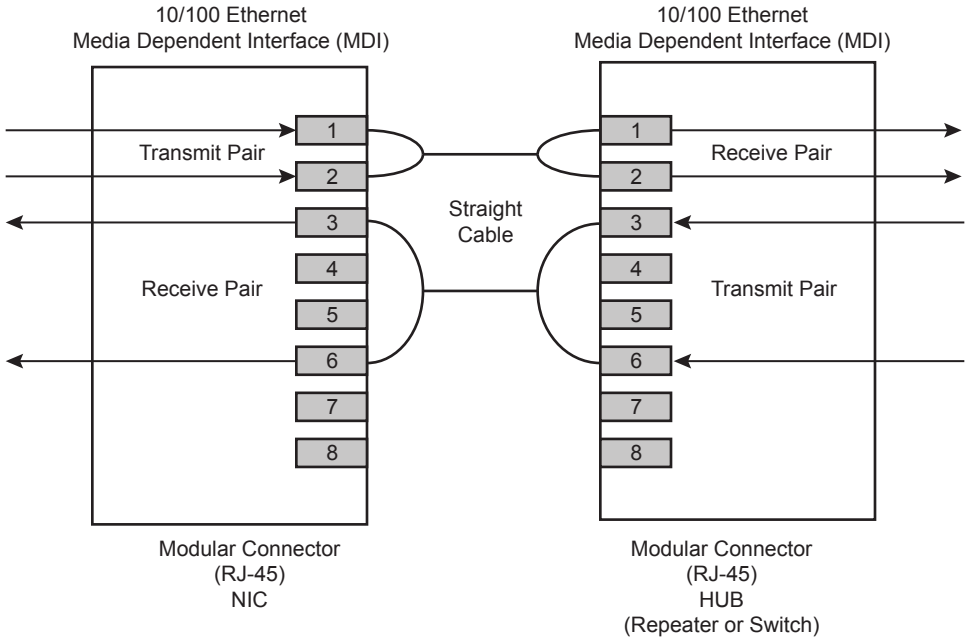


Figure 6. Typical Straight Cable Connection

6.16.2. Crossover Cable

A crossover cable connects a MDI device to another MDI device, or a MDI-X device to another MDI-X device. Figure 7 depicts a typical crossover cable connection between two switches or hubs (two MDI-X devices).

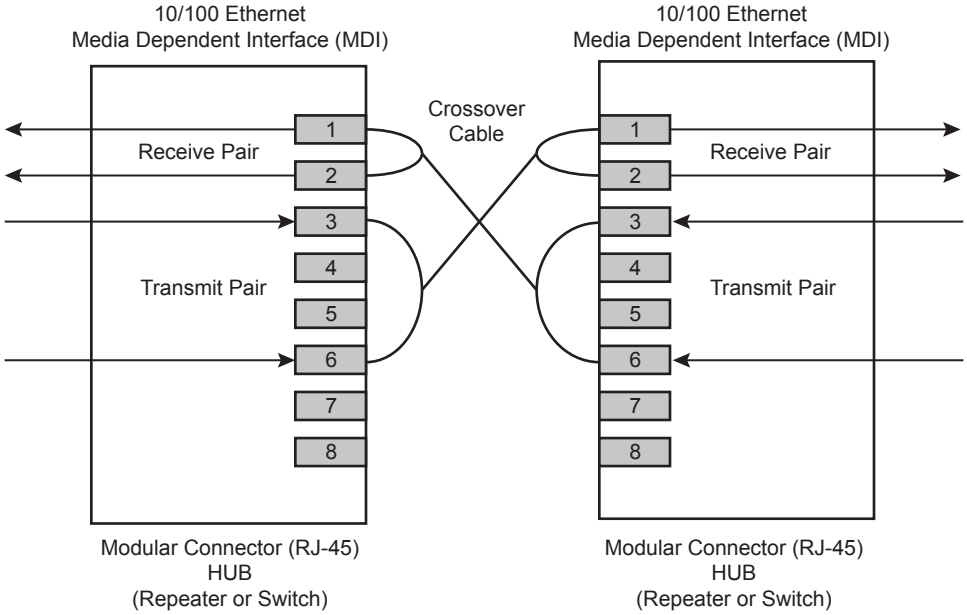


Figure 7. Typical Crossover Cable Connection

6.17. Reference Clock Connection Options

A crystal or external clock source, such as an oscillator, provides the reference clock for the HI-5200. Figure 8 illustrates how to connect the 25MHz reference clock for MII mode.

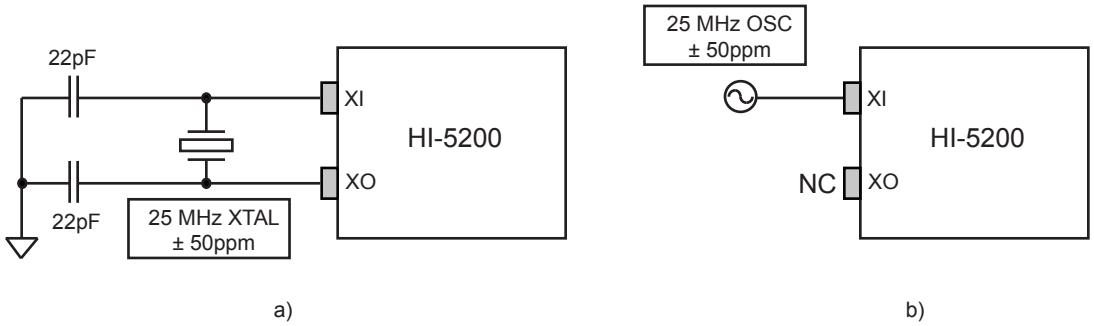


Figure 8. a) 25MHz Crystal or b) 25MHz Oscillator Reference Clock for HI-5200 MII Mode

Figure 9 illustrates how to connect the 50MHz reference clock for RMII mode (see also Figure 5).

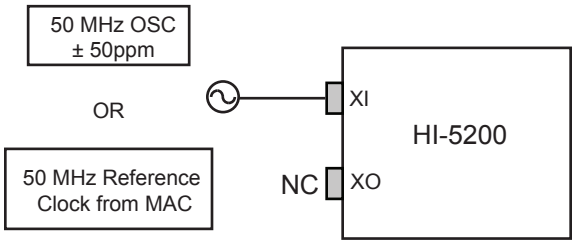


Figure 9. 50MHz Reference Clock for HI-5200 RMII Mode

7. Power Management

The HI-5200 power-management modes are described in the following sections.

7.1. Power Saving Mode

This mode is used to reduce power consumption when the cable is unplugged. It is in effect when auto-negotiation mode is enabled, cable is disconnected, and register 1Fh bit 10 is set to 1. Under power saving mode, the device shuts down all transceiver blocks, except for transmitter, energy detect and PLL circuits. Additionally, in MII mode, the RXC clock output is disabled. RXC clock is enabled after the cable is connected and link is established.

Power-saving mode is disabled by writing a zero to register 1Fh bit 10.

7.2. Power-Down Mode

This mode is used to power down the entire device when it is not in use. Power down mode is enabled by writing a one to register 0h bit 11. In the power down state, the HI-5200 disables all internal functions, except for the MII management interface.

7.3. Reference Circuit for Power and Ground Connections

The HI-5200 is a single 3.3V supply device with a built-in 1.8V low-noise regulator. The power and ground connections are shown in Figure 10 and Table 7.

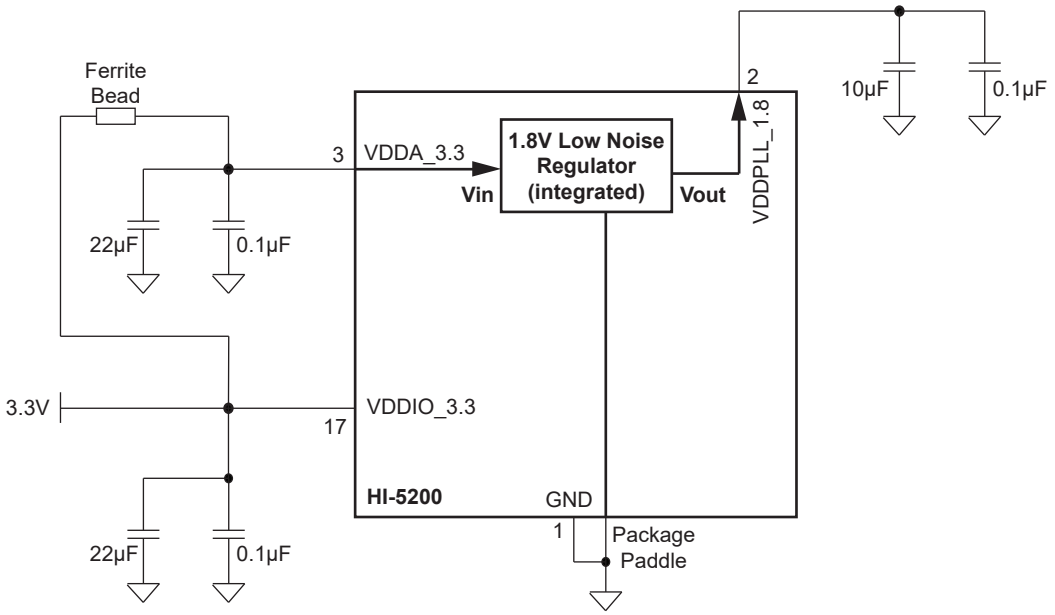


Figure 10. HI-5200 Power and Ground Connections

Table 7. HI-5200 Power and Ground Connections

Power Pin	Pin Number	Description
VDDPLL_1.8	2	Decouple with 10µF and 0.1µF capacitors to ground.
VDDA_3.3	3	Connect to board's 3.3V supply through ferrite bead.
VDDIO_3.3	17	Connect to board's 3.3V supply.
GND	1	Connect to Ground.
PACKAGE PADDLE	-	Connect to Ground.

8. Register Map

Register Number (Hex)	Description
0h	Basic Control
1h	Basic Status
2h	PHY Identifier 1
3h	PHY Identifier 2
4h	Auto-Negotiation Advertisement
5h	Auto-Negotiation Link Partner Ability
6h	Auto-Negotiation Expansion
7h	Auto-Negotiation Next Page
8h	Link Partner Next Page Ability
9h − 13h	Reserved
14h	MII Control
15h	RXER Counter
16h − 1Ah	Reserved
1Bh	Interrupt Control/Status
1Ch − 1Dh	Reserved
lEh	PHY Control 1
1Fh	PHY Control 2

9. Register Description

9.1. Register 0h – Basic Control

Bit No.	*Bit Name*	*Description*	*Mode[1]*	*Default*
15	Reset	1 = Software reset 0 = Normal operation This bit is self-cleared after a '1' is written to it.	RW/SC	0
14	Loop-Back	1 = Loop-back mode 0 = Normal operation	RW	0
13	Speed Select (LSB)	1 = 100Mbps 0 = 10Mbps. This bit is ignored if auto-negotiation is enabled (register 0h, bit 12 = 1).	RW	Set by SPEED strapping pin. See "Strapping Options" for details.
12	Auto-Negotiation Enable	1 = Enable auto-negotiation process 0 = Disable auto-negotiation process If enabled, auto-negotiation result overrides settings in register 0h, bit13 and 0h bit 8.	RW	Set by NWAYEN strapping pin. See "Strapping Options" for details.
11	Power Down	1 = Power-down mode 0 = Normal operation	RW	0
10	Isolate	1 = Electrical isolation of PHY from MII and TX+/TX- 0 = Normal operation	RW	Set by ISO strapping pin. See "Strapping Options" for details.
9	Restart Auto-Negotiation	1 = Restart auto-negotiation process 0 = Normal operation. This bit is self-cleared after a '1' is written to it.	RW/SC	0
8	Duplex Mode	1 = Full-duplex 0 = Half-duplex	RW	Inverse of DUPLEX strapping pin value. See "Strapping Options" for details.
7	Collision Test	1 = Enable COL test 0 = Disable COL test	RW	0
6 – 1	Reserved	–	RO	000_000
0	Disable Transmitter	0 = Enable transmitter 1 = Disable transmitter	RW	0

Notes:

1. RW = Read/Write. RO = Read only.
   SC = Self-cleared.
   LH = Latch high. LL = Latch low.

9.2. Register 1h – Basic Status

Bit No.	Bit Name	Description	Mode[1]	Default
15	100Base-T4	1 = T4 capable 0 = Not T4 capable	RO	0
14	100Base-TX Full Duplex	1 = Capable of 100Mbps full-duplex 0 = Not capable of 100Mbps full- duplex	RO	1
13	100Base-TX Half Duplex	1 = Capable of 100Mbps half-duplex 0 = Not capable of 100Mbps half- duplex	RO	1
12	10Base-T Full Duplex	1 = Capable of 10Mbps full-duplex 0 = Not capable of 10Mbps full- duplex	RO	1
11	10Base-T Half Duplex	1 = Capable of 10Mbps half-duplex 0 = Not capable of 10Mbps half- duplex	RO	1
10 – 7	Reserved	–	RO	0000
6	No Preamble	1 = Preamble suppression 0 = Normal preamble	RO	1
5	Auto-Negotiation Complete	1 = Auto-negotiation process completed 0 = Auto-negotiation process not completed	RO	0
4	Remote Fault	1 = Remote fault 0 = No remote fault	RO/LH	0
3	Auto-Negotiation Ability	1 = Capable to perform auto-negotiation 0 = Not capable to perform auto-negotiation	RO	1
2	Link Status	1 = Link is up 0 = Link is down	RO/LL	0
1	Jabber Detect	1 = Jabber detected 0 = Jabber not detected (default is low)	RO/LH	0
0	Extended Capability	1 = Supports extended capabilities registers	RO	1

9.3. Register 2h – PHY Identifier 1

Bit No.	Bit Name	Description	Mode[1]	Default
15 – 0	PHY ID Number	Assigned to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI). Kendin Communication's OUI is 0010A1 (hex)	RO	0022h

Notes:

1. RW = Read/Write. RO = Read only.
   SC = Self-cleared.
   LH = Latch high. LL = Latch low.

9.4. Register 3h – PHY Identifier 2

Bit No.	Bit Name	Description	Mode[1]	Default
15 – 10	PHY ID Number	Assigned to the 19th through 24th bits of the Organizationally Unique Identifier (OUI). Kendin Communication's OUI is 0010A1 (hex)	RO	0001_01
9 – 4	Model Number	Six bit manufacturer's model number	RO	01_0001
3 – 0	Revision Number	Four bit manufacturer's revision number	RO	Indicates silicon revision

Notes:

1. RW = Read/Write. RO = Read only.
   SC = Self-cleared.
   LH = Latch high. LL = Latch low.

9.5. Register 4h – Auto-Negotiation Advertisement

Bit No.	Bit Name	Description	Mode[1]	Default
15	Next Page	1 = Next page capable 0 = No next page capability.	RW	0
14	Reserved	–	RO	0
13	Remote Fault	1 = Remote fault supported 0 = No remote fault	RW	0
12	Reserved	–	RO	0
11 – 10	Pause	[00] = No PAUSE [10] = Asymmetric PAUSE [01] = Symmetric PAUSE [11]= Asymmetric & Symmetric PAUSE	RW	00
9	100Base-T4	1 = T4 capable 0 = No T4 capability	RO	0
8	100Base-TX Full-Duplex	1 = 100Mbps full-duplex capable 0 = No 100Mbps full-duplex capability	RW	Set by SPEED strapping pin. See "Strapping Options" for details.
7	100Base-TX Half-Duplex	1 = 100Mbps half-duplex capable 0 = No 100Mbps half-duplex capability	RW	Set by SPEED strapping pin. See "Strapping Options" for details.
6	10Base-T Full-Duplex	1 = 10Mbps full-duplex capable 0 = No 10Mbps full-duplex capability	RW	1

Bit No.	Bit Name	Description	Mode[1]	Default
5	10Base-T Half-Duplex	1 = 10Mbps half-duplex capable 0 = No 10Mbps half-duplex capability	RW	1
4 – 0	Selector Field	[00001] = IEEE 802.3	RW	0_0001

9.6. Register 5h – Auto-Negotiation Link Partner Ability

Bit No.	Bit Name	Description	Mode[1]	Default
15	Next Page	1 = Next page capable 0 = No next page capability	RO	0
14	Acknowledge	1 = Link code word received from partner 0 = Link code word not yet received	RO	0
13	Remote Fault	1 = Remote fault detected 0 = No remote fault	RO	0
12	Reserved	–	RO	0
11 – 10	Pause	[00] = No PAUSE [10]= Asymmetric PAUSE [01] = Symmetric PAUSE [11]= Asymmetric & Symmetric PAUSE	RO	00
9	100Base-T4	1 = T4 capable 0 = No T4 capability	RO	0
8	100Base-TX Full-Duplex	1 = 100Mbps full-duplex capable 0 = No 100Mbps full-duplex capability	RO	0
7	100Base-TX Half-Duplex	1 = 100Mbps half-duplex capable 0 = No 100Mbps half-duplex capability	RO	0
6	10Base-T Full-Duplex	1 = 10Mbps full-duplex capable 0 = No 10Mbps full-duplex capability	RO	0
5	10Base-T Half-Duplex	1 = 10Mbps half-duplex capable 0 = No 10Mbps half-duplex capability	RO	0
4 – 0	Selector Field	[00001] = IEEE 802.3	RO	0_0001

Notes:

1. RW = Read/Write. RO = Read only.
   SC = Self-cleared.
   LH = Latch high. LL = Latch low.

9.7. Register 6h – Auto-Negotiation Expansion

Bit No.	Bit Name	Description	Mode[1]	Default
15 – 5	Reserved	–	RO	0000_0000_000
4	Parallel Detection Fault	1 = Fault detected by parallel detection 0 = No fault detected by parallel detection.	RO/LH	0
3	Link Partner Next Page Able	1 = Link partner has next page capability 0 = Link partner does not have next page capability	RO	0
2	Next Page Able	1 = Local device has next page capability 0 = Local device does not have next page capability	RO	1
1	Page Received	1 = New page received 0 = New page not received yet	RO/LH	0
0	Link Partner Auto-Negotiation Able	1 = Link partner has auto-negotiation capability 0 = Link partner does not have auto-negotiation capability	RO	0

Notes:

1. RW = Read/Write. RO = Read only.
   SC = Self-cleared.
   LH = Latch high. LL = Latch low.

9.8. Register 7h – Auto-Negotiation Next Page

Bit No.	Bit Name	Description	Mode[1]	Default
15	Next Page	1 = Additional next page(s) will follow 0 = Last page	RW	0
14	Reserved	–	RO	0
13	Message Page	1 = Message page 0 = Unformatted page	RW	1
12	Acknowledge2	1 = Will comply with message 0 = Cannot comply with message	RW	0
11	Toggle	1 = Previous value of the transmitted link code word equaled logic one 0 = Logic zero	RO	0

Bit No.	Bit Name	Description	Mode[1]	Default
10 – 0	Message Field	11-bit wide field to encode 2048 messages	RW	000_0000_0001

Notes:

1. RW = Read/Write. RO = Read only.
   SC = Self-cleared.
   LH = Latch high. LL = Latch low.

9.9. Register 8h – Link Partner Next Page Ability

Bit No.	Bit Name	Description	Mode[1]	Default
15	Next Page	1 = Additional Next Page(s) will follow 0 = Last page	RO	0
14	Acknowledge	1 = Successful receipt of link word 0 = No successful receipt of link word	RO	0
13	Message Page	1 = Message page 0 = Unformatted page	RO	0
12	Acknowledge2	1 = Able to act on the information 0 = Not able to act on the information	RO	0
11	Toggle	1 = Previous value of transmitted link code word equal to logic zero 0 = Previous value of transmitted link code word equal to logic one	RO	0
10 – 0	Message Field		RO	000_0000_0000

Notes:

1. RW = Read/Write. RO = Read only.
   SC = Self-cleared.
   LH = Latch high. LL = Latch low.

9.10. Register 14h – MII Control

Bit No.	Bit Name	Description	Mode[1]	Default
15 – 8	Reserved	–	RO	0000_0000
7	100Base-TX Preamble Restore	1 = Restore received preamble to MII output (random latency) 0 = Consume 1-byte preamble before sending frame to MII output for fixed latency	RW	0 or 1 (if pins CONFIG[2:0] = 100) See “Strapping Options” for details.
6	10Base-T Preamble Restore	1 = Restore received preamble to MII output 0 = Remove all 7-bytes of preamble before sending frame (starting with SFD) to MII output	RW	
5 – 0	Reserved	–	RO	00_0001

Notes:

1. RW = Read/Write. RO = Read only.
   SC = Self-cleared.
   LH = Latch high. LL = Latch low.

9.11. Register 15h – RXER Counter

Bit No.	Bit Name	Description	Mode[1]	Default
15 – 0	RXER Counter	Receive error counter for Symbol Error frames	RO/SC	0000h

Notes:

1. RW = Read/Write. RO = Read only.
   SC = Self-cleared.
   LH = Latch high. LL = Latch low.

9.12. Register 1Bh – Interrupt Control/Status

Bit No.	*Bit Name*	*Description*	*Mode[1]*	*Default*
15	Jabber Interrupt Enable	1 = Enable Jabber Interrupt 0 = Disable Jabber Interrupt	RW	0
14	Receive Error Interrupt Enable	1 = Enable Receive Error Interrupt 0 = Disable Receive Error Interrupt	RW	0
13	Page Received Interrupt Enable	1 = Enable Page Received Interrupt 0 = Disable Page Received Interrupt	RW	0
12	Parallel Detect Fault Interrupt Enable	1 = Enable Parallel Detect Fault Interrupt 0 = Disable Parallel Detect Fault Interrupt	RW	0
11	Link Partner Acknowledge Interrupt Enable	1 = Enable Link Partner Acknowledge Interrupt 0 = Disable Link Partner Acknowledge Interrupt	RW	0
10	Link Down Interrupt Enable	1= Enable Link Down Interrupt 0 = Disable Link Down Interrupt	RW	0
9	Remote Fault Interrupt Enable	1 = Enable Remote Fault Interrupt 0 = Disable Remote Fault Interrupt	RW	0
8	Link Up Interrupt Enable	1 = Enable Link Up Interrupt 0 = Disable Link Up Interrupt	RW	0
7	Jabber Interrupt	1 = Jabber occurred 0 = Jabber did not occur	RO/SC	0
6	Receive Error Interrupt	1 = Receive Error occurred 0 = Receive Error did not occur	RO/SC	0
5	Page Receive Interrupt	1 = Page Receive occurred 0 = Page Receive did not occur	RO/SC	0
4	Parallel Detect Fault Interrupt	1 = Parallel Detect Fault occurred 0 = Parallel Detect Fault did not occur	RO/SC	0
3	Link Partner Acknowledge Interrupt	1= Link Partner Acknowledge occurred 0= Link Partner Acknowledge did not occur	RO/SC	0
2	Link Down Interrupt	1= Link Down occurred 0= Link Down did not occur	RO/SC	0
1	Remote Fault Interrupt	1= Remote Fault occurred 0= Remote Fault did not occur	RO/SC	0

Bit No.	Bit Name	Description	Mode[1]	Default
0	Link Up Interrupt	1= Link Up occurred 0= Link Up did not occur	RO/SC	0

Notes:

1. RW = Read/Write. RO = Read only.
   SC = Self-cleared.
   LH = Latch high. LL = Latch low.

9.13. Register 1Eh – PHY Control 1

Bit No.	Bit Name	Description	Mode[1]	Default
15 – 14	LED Mode	[00] = LED1: Speed LED0: Link/Activity [01] = LED1: Activity LED0: Link [10], [11] = Reserved	RW	00 See “Table 1. HI-5200 Pin Descriptions”, pins 30, 31.
13	Polarity	0 = Polarity is not reversed 1 = Polarity is reversed	RO	
12	Reserved	–	RO	0
11	MDI/MDI-X State	0 = MDI 1 = MDI-X	RO	
10 – 8	Reserved			
7	Remote loopback	0 = Normal mode 1 = Remote (analog) loop back is enabled	RW	0
6 – 0	Reserved			

Notes:

1. RW = Read/Write. RO = Read only.
   SC = Self-cleared.
   LH = Latch high. LL = Latch low.

9.14. Register 1Fh – PHY Control 2

Bit No.	*Bit Name*	*Description*	*Mode[1]*	*Default*
15	HP_MDIX	0 = Micrel Auto MDI/MDI-X mode 1 = HP Auto MDI/MDI-X mode	RW	1
14	MDI/MDI-X Select	When Auto MDI/MDI-X is disabled, 0 = MDI Mode Transmit on TX+/- (pins 7, 6) and Receive on RX+/- (pins 5, 4) 1 = MDI-X Mode Transmit on RX+/- (pins 5,4) and Receive on TX+/- (pins 7, 6)	RW	0
13	Pair Swap Disable	1 = Disable auto MDI/MDI-X 0 = Enable auto MDI/MDI-X	RW	0
12	Energy Detect	1 = Presence of signal on RX+/- analog wire pair 0 = No signal detected on RX+/-	RO	0
11	Force Link	1 = Force link pass 0 = Normal link operation This bit bypasses the control logic and allows transmitter to send pattern even if there is no link.	RW	0
10	Power Saving	1 = Enable power saving 0 = Disable power saving If power saving mode is enabled and the cable is disconnected, the RXC clock output (in MII mode) is disabled. RXC clock is enabled after the cable is connected and link is established.	RW	0
9	Interrupt Level	1 = Interrupt pin active high 0 = Interrupt pin active low	RW	0
8	Enable Jabber	1 = Enable jabber counter 0 = Disable jabber counter	RW	1
7	Auto-Negotiation Complete	1 = Auto-negotiation process completed 0 = Auto-negotiation process not completed	RW	0
6	Enable Pause (Flow Control)	1 = Flow control capable 0 = No flow control capability	RO	0
5	PHY Isolate	1 = PHY in isolate mode 0 = PHY in normal operation	RO	0

Bit No.	*Bit Name*	*Description*	*Mode[1]*	*Default*
4 – 2	Operation Mode Indication	[000] = Still in auto-negotiation [001] = 10Base-T half-duplex [010] = 100Base-TX half-duplex [011] = Reserved [101] = 10Base-T full-duplex [110] = 100Base-TX full-duplex [111] = Reserved	RO	000
1	Enable SQE test	1 = Enable SQE test 0 = Disable SQE test	RW	0
0	Disable Data Scrambling	1 = Disable scrambler 0 = Enable scrambler	RW	0

Notes:

1. RW = Read/Write. RO = Read only.
   SC = Self-cleared.
   LH = Latch high. LL = Latch low.

10. Absolute Maximum Ratings[1]

Supply Voltage	$V_{DDPLL\_1.8}$	− 0.5V to + 2.4V
	$V_{DDIO\_3.3}$, $V_{DDA\_3.3}$	− 0.5V to + 4.0V
Input Voltage (all inputs)		− 0.5V to + 4.0V
Output Voltage (all outputs)		− 0.5V to + 4.0V
Lead Temperature (soldering 10s)		260°C
Storage Temperature (Ts)		− 55°C to + 150°C
ESD Rating[2]		6kV

11. Operating Ratings[3]

Supply Voltage, $V_{DDIO\_3.3}$, $V_{DDA\_3.3}$		+ 3.135V to + 3.465V
Ambient Temperature (T_A)	Enhanced	− 40°C to + 105°C
	Extended	− 55°C to + 125°C
Maximum Case Temperature (T_C maximum)		150°C
Junction-to-Ambient Thermal Resistance (θ_{JA})		34°C/W
Junction-to-Case Thermal Resistance (θ_{JC})		6°C/W

Notes:

1. Exceeding the absolute maximum rating may damage the device. Stresses greater than the absolute maximum rating may cause permanent damage to the device. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.
2. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5kΩ in series with 100pF.
3. The device is not guaranteed to function outside its operating rating.

12. Electrical Characteristics[1]

Parameters	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Supply Current[2]						
100Base-TX	I_{DD1}	Chip only (no transformer); Full-duplex traffic @ 100% utilization		53.0		mA
10Base-T	I_{DD2}	Chip only (no transformer); Full-duplex traffic @ 100% utilization		38.0		mA
Power-Saving Mode	I_{DD3}	Ethernet cable disconnected (Register 1Fh, bit 10 = 1)		32.0		mA
Power-Down Mode	I_{DD4}	Software power-down (Register 0h, bit 11 = 1)		4.0		mA
TTL Inputs						
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Input Current	I_{IN}	VIN = GND ~ VDDIO		−10	+10	µA
TTL Outputs						
Output High Voltage	V_{OH}	I_{OH} = −4mA	2.4			V
Ouput Low Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
Output Tri-State Leakage	$\|I_{OZ}\|$				10	µA
LED Outputs						
Output Drive Current	I_{LED}	Each LED pin (LED0, LED1)		8.0		mA
100Base-TX Transmit (measured differentially after 1:1 transformer)						
Peak Differential Output Voltage	V_O	100Ω termination across differential output	0.95		1.05	V
Output Voltage Imbalance	V_{IMB}	100Ω termination across differential output			2	%
Rise/Fall Time	t_r, t_f		3		5	ns
Rise/Fall Time Imbalance			0		0.5	ns
Duty Cycle Distortion					±0.25	ns
Overshoot					5	%
Reference Voltage of ISET	V_{SET}			0.65		V
Output Jitter		Peak-to-peak		0.7	1.4	ns
10Base-T Transmit (measured differentially after 1:1 transformer)						
Peak Differential Output Voltage	V_P	100Ω termination across differential output	2.2		2.8	V

Parameters	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Jitter Added		Peak-to-peak			3.5	ns
Rise/Fall Time	t_r, t_f			25		ns
10Base-T Receive						
Squelch Threshold	V_{SQ}	5MHz square wave		400		mV

Notes:

1. TA = 25°C. Specification for packaged product only.
2. Current consumption is for the single 3.3V supply HI-5200 device only, and includes the 1.8V supply voltage (VDDPLL_1.8) that is provided by the HI-5200. The PHY port's transformer consumes an additional 45mA @ 3.3V for 100Base-TX and 70mA @ 3.3V for 10Base-T.

12.1. Recommended Transformer Characteristics

A 1:1 isolation transformer is required at the line interface. An isolation transformer with integrated common-mode chokes is recommended for exceeding FCC requirements. Recommended transformer characteristics are shown below.

Parameters	Test Conditions	Value			Unit
		Min	Typ	Max	
Turns Ratio		1 CT : 1 CT			
Open-Circuit Inductance (minimum)	100mV, 100kHz, 8mA	350			µH
Leakage Inductance (maximum)	1MHz (minimum)			0.4	µH
Inter-Winding Capacitance (typical)			12.0		pF
DC Resistance (typical)			0.9		Ω
Insertion Loss (maximum)	0MHz – 65MHz			-1.0	dB
HIPOT (minimum)		1500			V_{RMS}

12.2. Typical Reference Crystal Characteristics

Parameters	Test Conditions	Value			Unit
		Min	Typ	Max	
Frequency			25		MHz
Frequency Tolerance (maximum)				±50	ppm
Load Capacitance			20		pF
Series Resistance			40		Ω

13. Timing Diagrams

13.1. MII Timing

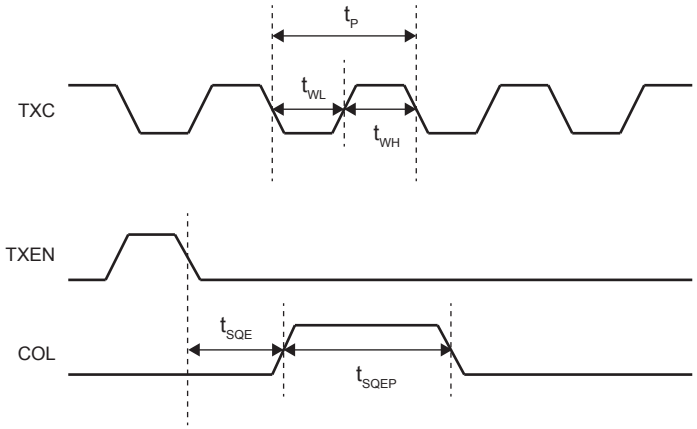


Figure 11. MII SQE Timing (10Base-T)

Table 8. MII SQE Timing (10Base-T) Parameters

Timing Parameter	Symbol	Min	Typ	Max	Unit
TXC Period	t_P		400		ns
TXC Pulse Width Low	t_{WL}		200		ns
TXC Pulse Width High	t_{WH}		200		ns
COL (SQE) Delay After TXEN De-Asserted	t_{SQE}		2.5		µs
COL (SQE) Pulse Duration	t_{SQEP}		1.0		µs

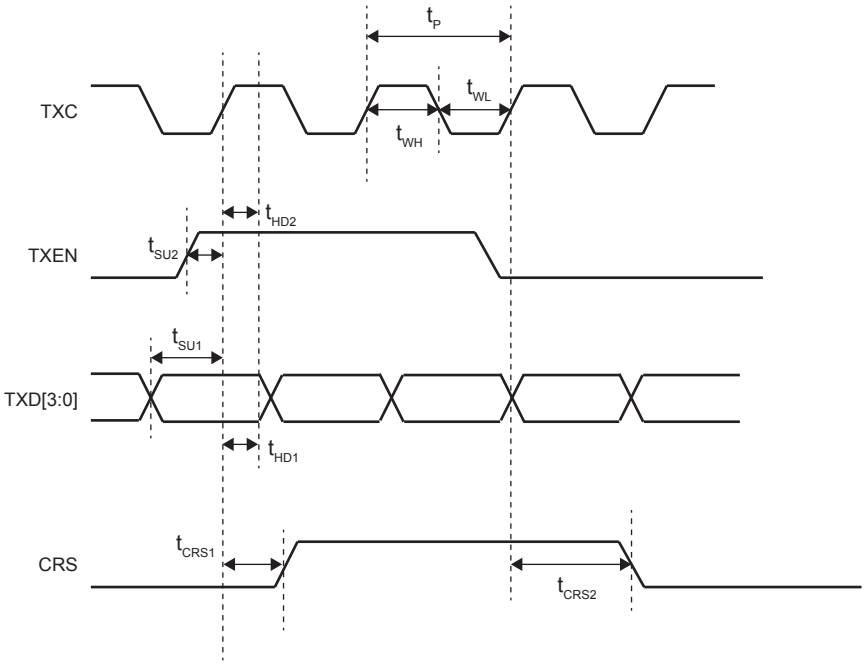


Figure 12. MII Transmit Timing (10Base-T)

Table 9. MII Transmit Timing (10Base-T) Parameters

Timing Parameter	Symbol	Min	Typ	Max	Unit
TXC Period	t_P		400		ns
TXC Pulse Width Low	t_{WL}		200		ns
TXC Pulse Width High	t_{WH}		200		ns
TXD[3:0] Setup to Rising Edge of TXC	t_{SU1}	10			ns
TXEN Setup to Rising Edge of TXC	t_{SU2}	10			ns
TXD[3:0] Hold from Rising Edge of TXC	t_{HD1}	0			ns
TXEN Hold from Rising Edge of TXC	t_{HD2}	0			ns
TXEN High to CRS Asserted Latency	t_{CRS1}		160		ns
TXEN Low to CRS De-Asserted Latency	t_{CRS2}		510		ns

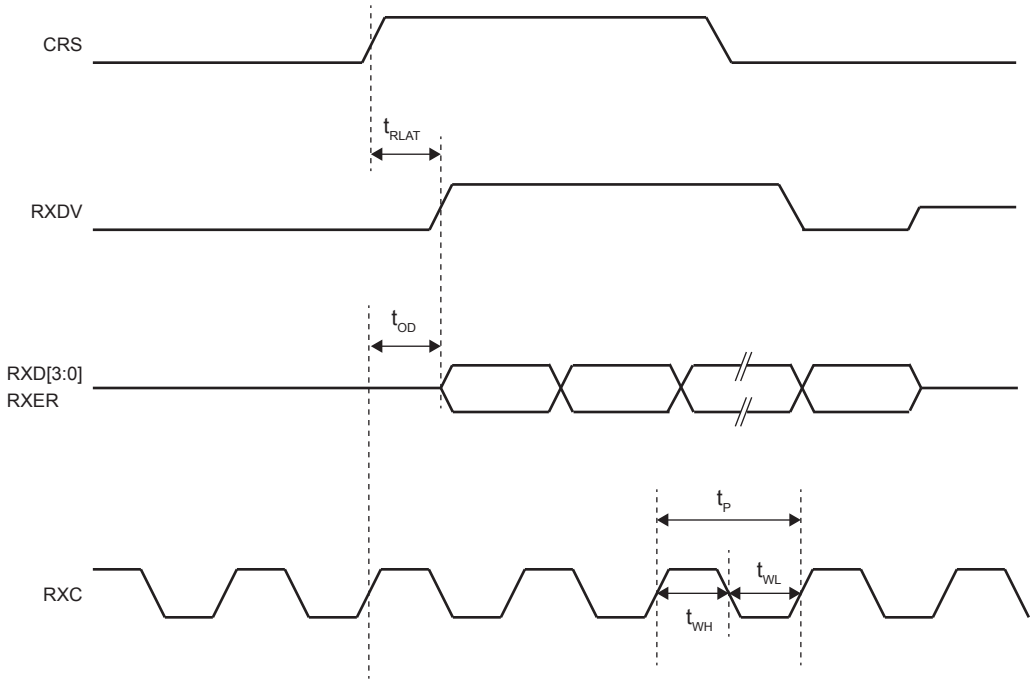


Figure 13. MII Receive Timing (10Base-T)

Table 10. MII Receive Timing (10Base-T) Parameters

Timing Parameter	Symbol	Min	Typ	Max	Unit
RXC Period	t_P		400		ns
RXC Pulse Width Low	t_{WL}		200		ns
RXC Pulse Width High	t_{WH}		200		ns
(RXD[3:0], RXER, RXDV) Output Delay from Rising Edge of RXC	t_{OD}	182		225	ns
CRS to (RXD[3:0], RXER, RXDV) Latency	t_{RLAT}		6.5		µs

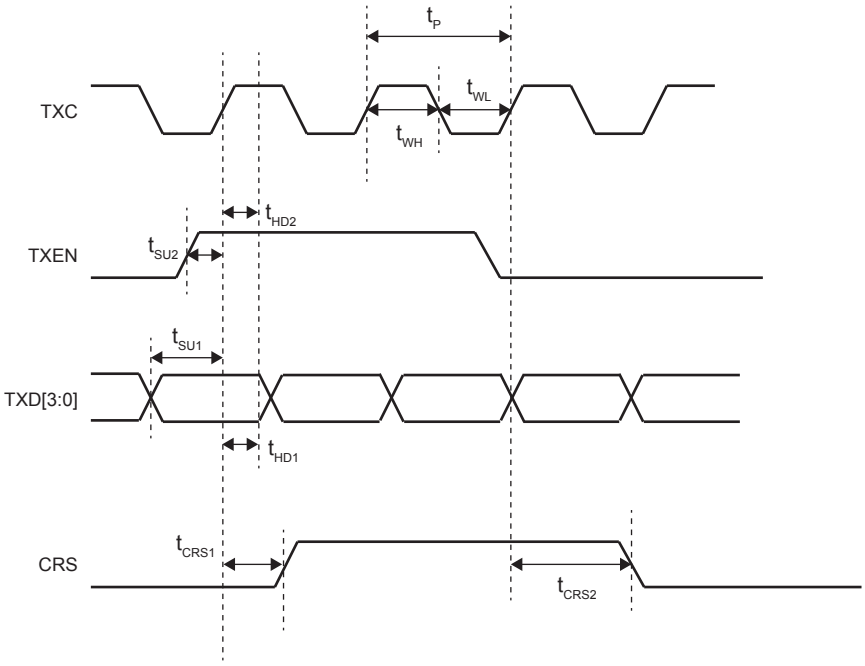


Figure 14. MII Transmit Timing (100Base-Tx)

Table 11. MII Transmit Timing (100Base-Tx) Parameters

Timing Parameter	Symbol	Min	Typ	Max	Unit
TXC Period	t_P		40		ns
TXC Pulse Width Low	t_{WL}		20		ns
TXC Pulse Width High	t_{WH}		20		ns
TXD[3:0] Setup to Rising Edge of TXC	t_{SU1}	10			ns
TXEN Setup to Rising Edge of TXC	t_{SU2}	10			ns
TXD[3:0] Hold from Rising Edge of TXC	t_{HD1}	0			ns
TXEN Hold from Rising Edge of TXC	t_{HD2}	0			ns
TXEN High to CRS Asserted Latency	t_{CRS1}		34		ns
TXEN Low to CRS De-Asserted Latency	t_{CRS2}		33		ns

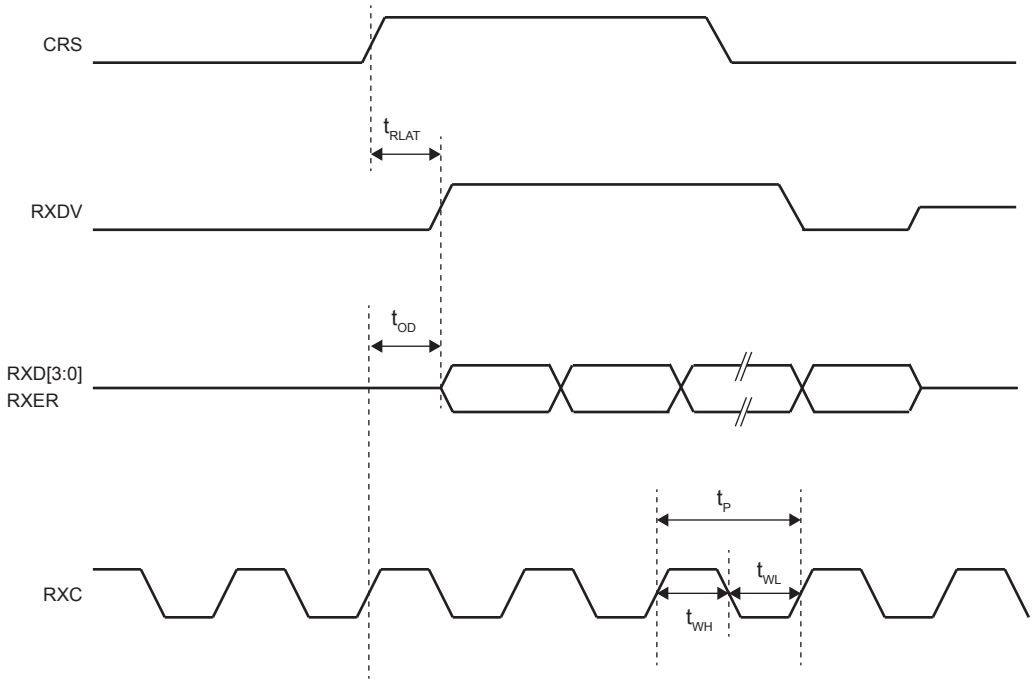


Figure 15. MII Receive Timing (100Base-Tx)

Table 12. MII Receive Timing (100Base-Tx) Parameters

Timing Parameter	Symbol	Min	Typ	Max	Unit
RXC Period	t_P		40		ns
RXC Pulse Width Low	t_{WL}		20		ns
RXC Pulse Width High	t_{WH}		20		ns
(RXD[3:0], RXER, RXDV) Output Delay from Rising Edge of RXC	t_{OD}	19		25	ns
CRS to RXDV Latency	t_{RLAT}		140		ns
CRS to RXD[3:0] Latency			52		ns
CRS to RXER Latency			60		ns

13.2. RMII Timing

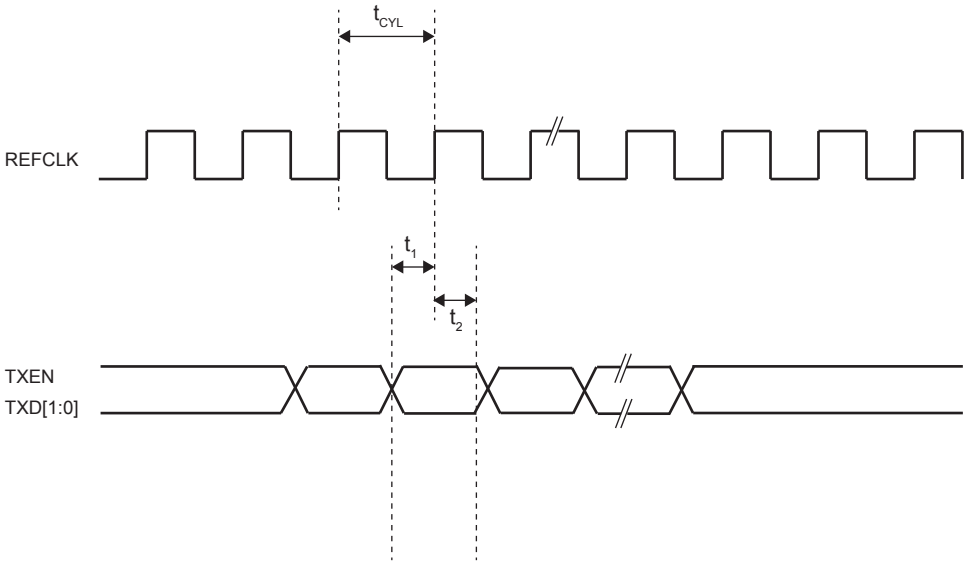


Figure 16. RMII Transmit Timing

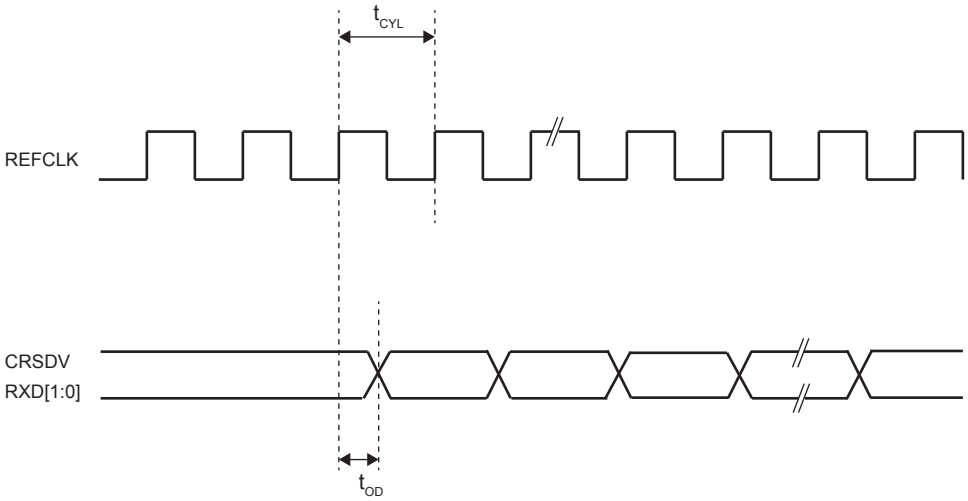


Figure 17. RMII Receive Timing

Table 13. RMII Timing Parameters

Timing Parameter	Symbol	Min	Typ	Max	Unit
Clock Cycle	t_{CYL}		20		ns
Setup Time	t_1	4			ns
Hold Time	t_2	2			ns
Output Delay	t_{OD}	3		9	ns

13.3. Auto-Negotiation Timing

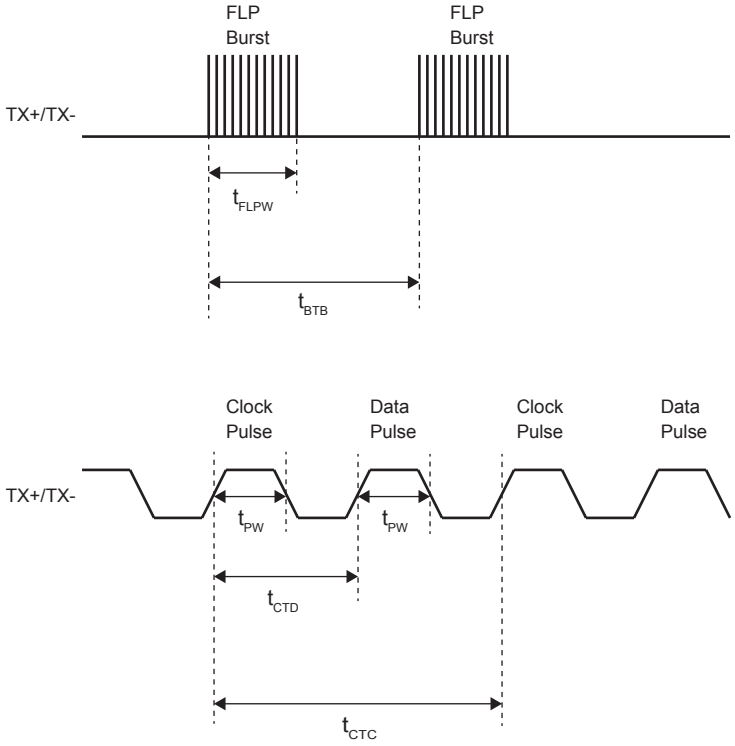


Figure 18. Auto-Negotiation Fast Link Pulse (FLP) Timing

Table 14. Auto-Negotiation Fast Link Pulse (FLP) Timing Parameters

Timing Parameter	Symbol	Min	Typ	Max	Unit
FLP Burst to FLP Burst	t_{BTB}	8	16	24	ms
FLP Burst Width	t_{FLPW}		2		ms
Clock/Data Pulse Width	t_{PW}		100		ns
Clock Pulse to Data Pulse	t_{CTD}	55.5	64	69.5	µs
Clock Pulse to Clock Pulse	t_{CTC}	111	128	139	µs
Number of Clock/Data Pulse per FLP Burst		17		33	

13.4. MDC/MDIO Timing

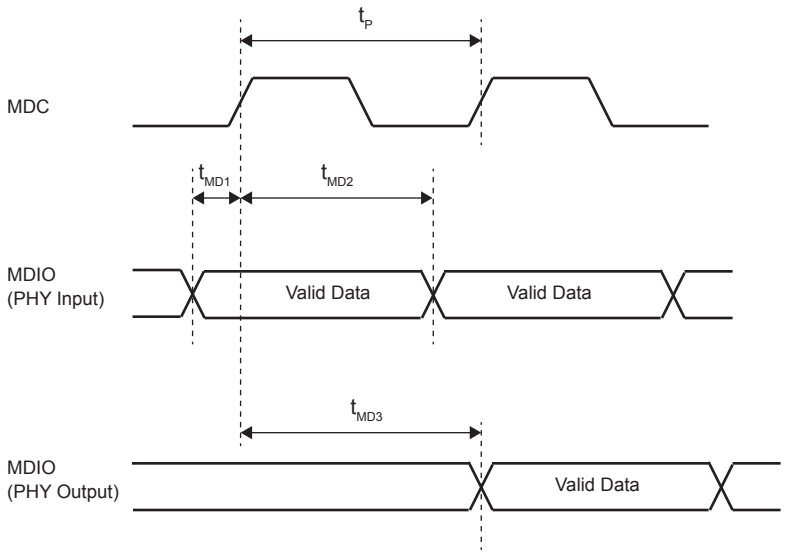


Figure 19. MDC/MDIO Timing

Table 15. MDC/MDIO Timing Parameters

Timing Parameter	Symbol	Min	Typ	Max	Unit
MDC Period	t_P		400		ns
MDIO (PHY Input) Setup to Rising Edge of MDC	t_{MD1}	10			ns
MDIO (PHY Input) Hold from Rising Edge of MDC	t_{MD2}	4			ns
MDIO (PHY Output) Delay from Rising Edge of MDC	t_{MD3}		222		ns

13.5. Power-Up/Reset Timing

The HI-5200 reset timing requirement is summarized in Figure 20 and Table 16.

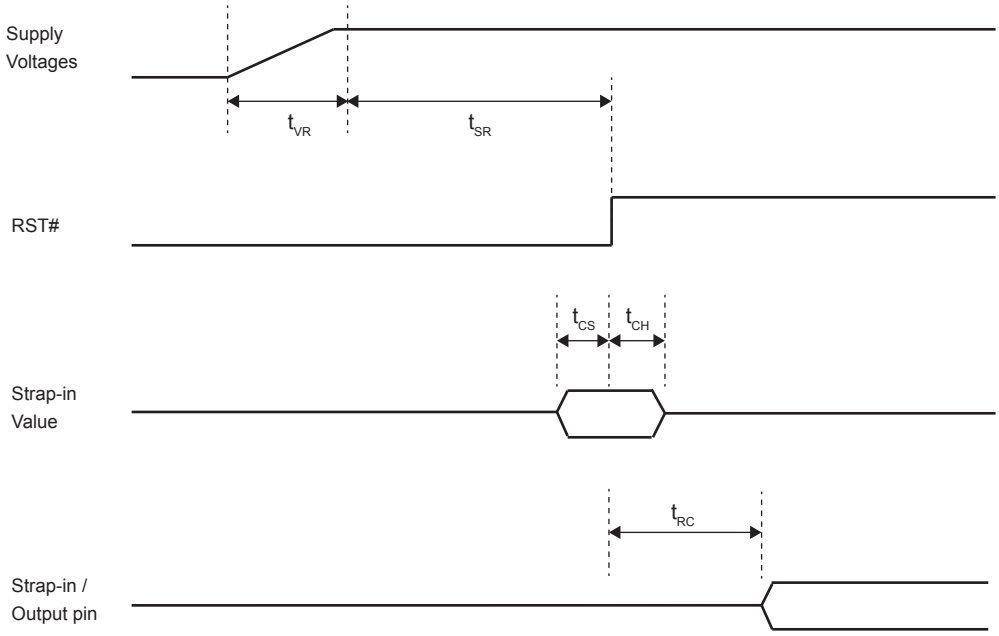


Figure 20. Power-Up/Reset Timing

Table 16. Power-Up/Reset Timing Parameters

Timing Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage ($V_{DDIO\_3.3}$, $V_{DDA\_3.3}$) Rise Time	t_{VR}	250			µs
Stable Supply Voltage to Reset High	t_{SR}	10			ms
Configuration Setup Time	t_{CS}	5			ns
Configuration Hold Time	t_{CH}	5			ns
Reset to Strap-In Pin Output	t_{RC}	6			ns

The supply voltage ($V_{DDIO\_3.3}$ and $V_{DDA\_3.3}$) power-up waveform should be monotonic. The 250µs minimum rise time is from 10% to 90%.

After the de-assertion of reset, it is recommended to wait a minimum of 100µs before starting programming on the MIIM (MDC/MDIO) Interface.

14. Reset Circuits

The reset circuit in Figure 21 is recommended for powering up the HI-5200 if reset is triggered by the power supply.

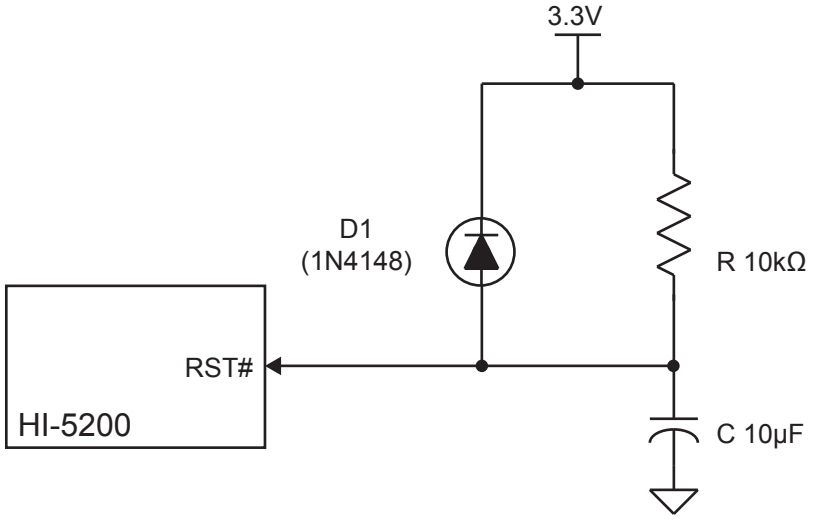


Figure 21. Recommended Reset Circuit

The reset circuit in Figure 22 is recommended for applications where reset is driven by another device (e.g., CPU or FPGA). At power-on-reset, R, C and D1 provide the necessary ramp rise time to reset the HI-5200. The RST_OUT_n from CPU/FPGA provides the warm reset after power-up.

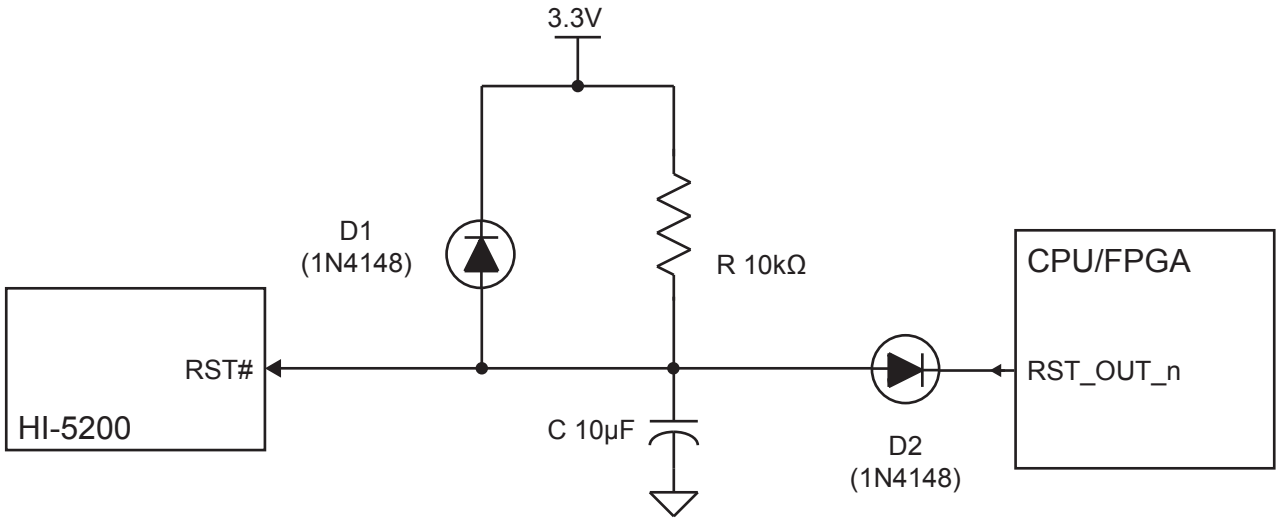


Figure 22. Recommended Reset Circuit for interfacing with CPU/FPGA Reset Output

15. Reference Circuits for LED Strapping Pins

Figure 23 shows the reference circuits for pull-up, float and pull-down on the LED1 and LED0 strapping pins.

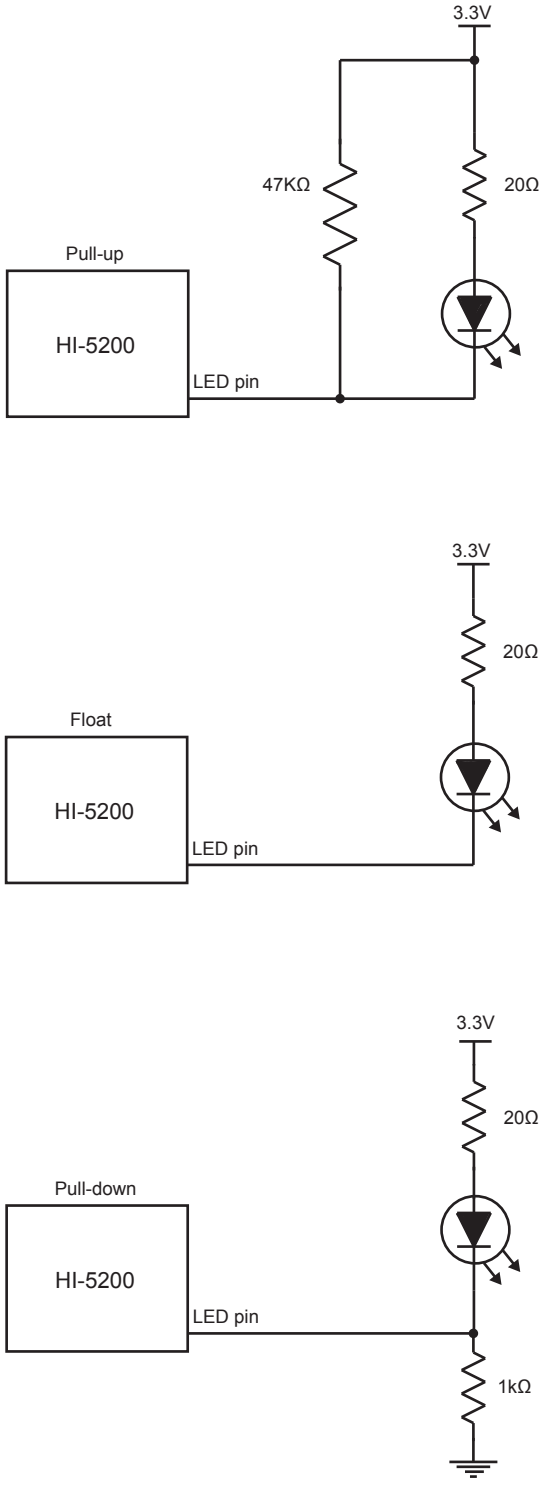


Figure 23. Reference Circuits for LED Strapping Pins

16. Recommended Single Port Magnetics

Manufacturer	Part Number	Turns Ratios	Auto MDI-X	Number of Ports	Operating Temperature
Premier Magnetics	PM-L6102A	1:1	Yes	1	− 40°C to + 105°C
Premier Magnetics	PM-L6102B	1:1	Yes	1	− 55°C to + 125°C

17. Ordering Information

HI-5200 Px x x

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
W	-40°C to +105°C (Enhanced)	W	No
T	-55°C to +125°C (Extended)	T	No
M	-55°C to +125°C (Extended with burn-in)	M	Yes

PART NUMBER	PACKAGE DESCRIPTION
PC	32 PIN PLASTIC CHIP-SCALE PACKAGE, 5 x 5mm QFN (32PCS)
PQ	32 PIN PLASTIC QUAD FLAT PACK, Thermally Enhanced EPQFP (32EPQ)

18. Revision History

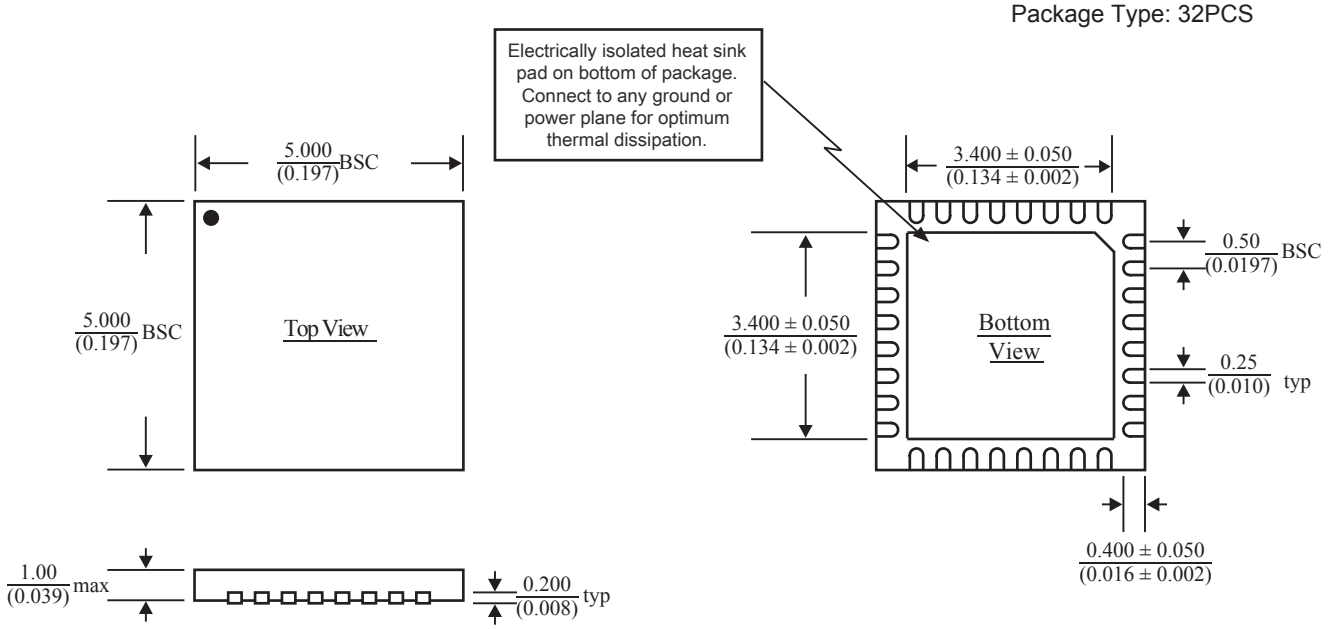
Revision	Date	Description of Change
DS5200, Rev. New	11/02/17	Initial Release
Rev. A	11/14/17	Change Enhanced temperature range from -40C – +95C to -40C – +105C
Rev. B	02/09/18	Replace QFP package (32PQS) with thermally enhanced QFP package (32EPQ). Packages are identical with the exception of the added exposed heatsink on 32EPQ.
Rev. C	04/27/18	Change title page format. Remove HI-5201 product variant.
Rev. D	05/24/18	Add “Recommended Single Port Magnetics” section.
Rev. E	01/10/2020	Add Premier Magnetics transformers to “Recommended Single Port Magnetics” section. Correct incorrect arrow in 32PCS package drawing.
Rev. F	08/19/2021	Correct typos in 1.8V supply recommended decoupling capacitors.

19. Package Dimensions

32-PIN PLASTIC CHIP-SCALE PACKAGE (QFN)

millimeters (inches)

Package Type: 32PCS

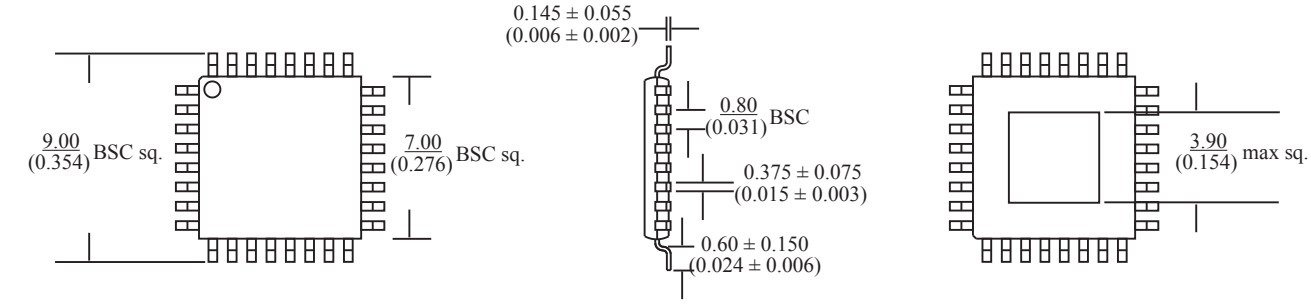


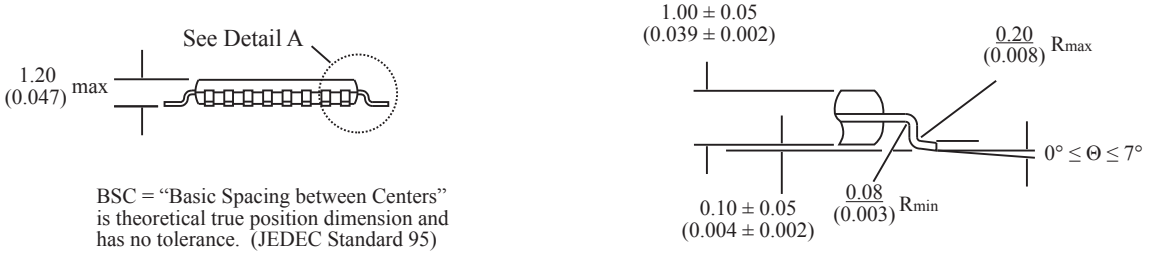
BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

32 PIN PLASTIC QUAD FLAT PACK (EPQFP)
(Thermally Enhanced)

millimeters (inches)

Package Type: 32EPQ





BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)